Parallel Architectures

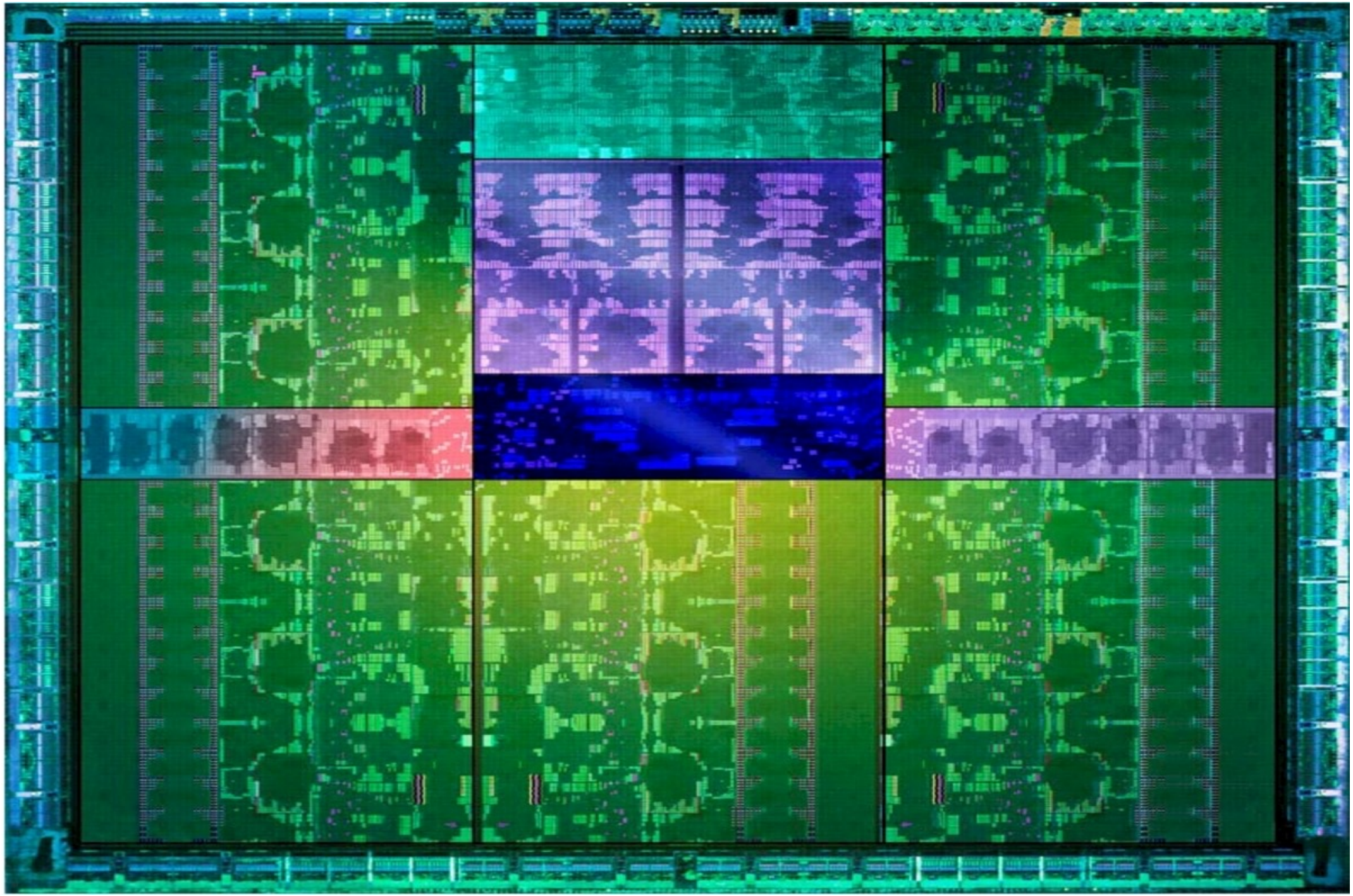
Chris Rossbach

Outline for Today

- Questions?
- Administrivia
  - Exam soon
- Agenda
  - Parallel Architectures (GPU background)

Faux Quiz questions

- What is hardware multi-threading; what problem does it solve?
- What is the difference between a vector processor and a scalar?
- Implement a parallel scan or reduction
- How are GPU workloads different from GPGPU workloads?
- How does SIMD differ from SIMT?
- List and describe some pros and cons of vector/SIMD architectures.
- GPUs historically have elided cache coherence.Why? What impact does it have on the the programmer?
- List some ways that GPUs use concurrency but not necessarily parallelism.



A modern GPU: Volta V100

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  - Streaming Multiprocessor

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Also:
CU or *ACE*

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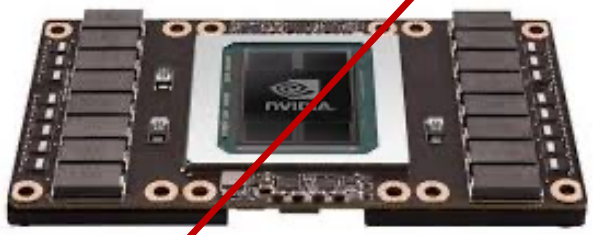

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  - 64 cores/SM
  - 5210 threads!
  - 15.7 TFLOPS

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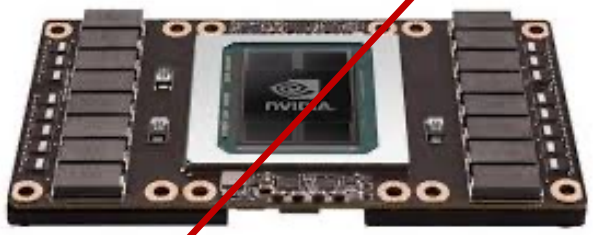

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Roughly: all of pfxsum 1,000s X/sec

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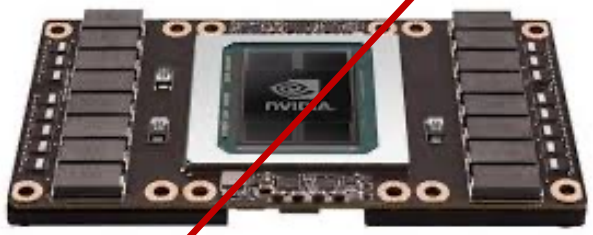

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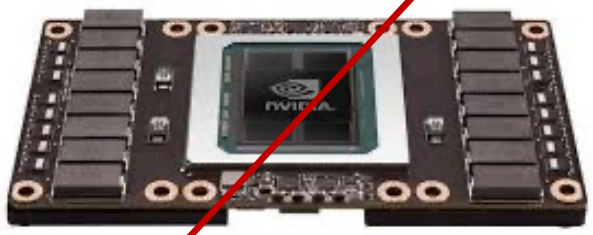

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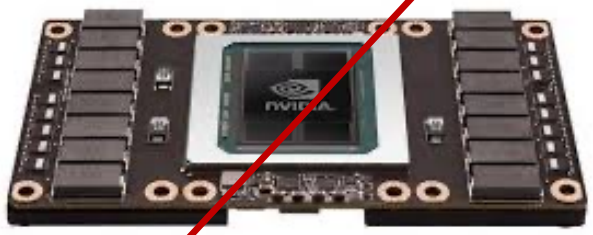

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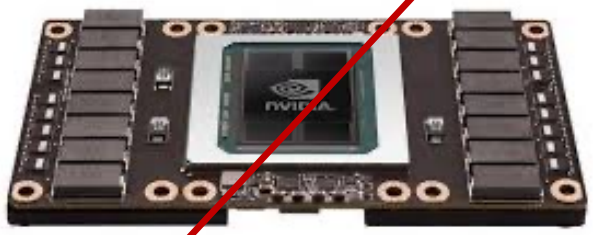

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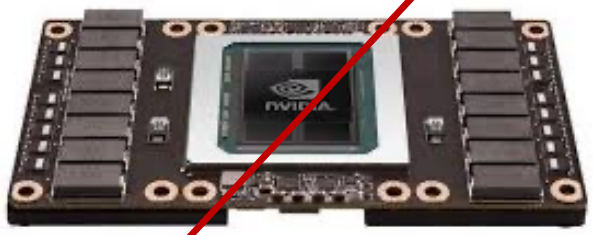

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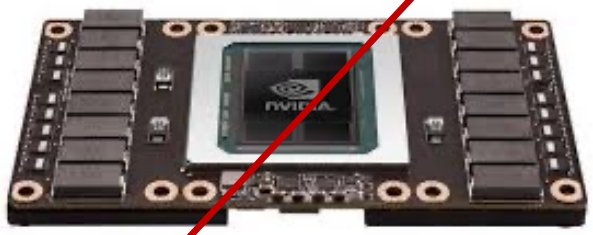

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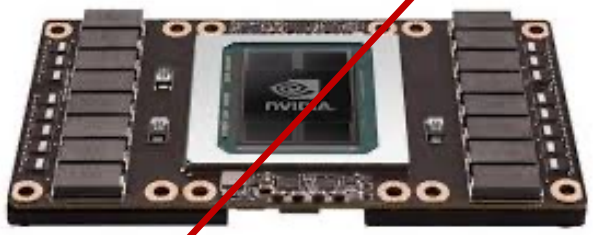

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How do you program a machine like this? pthread_create()?

GPUs: Outline

- Background from many areas
  - Architecture
    - Vector processors
    - Hardware multi-threading
  - Graphics
    - Graphics pipeline
    - Graphics programming models
  - Algorithms
    - parallel architectures → parallel algorithms
- Programming GPUs
  - CUDA
  - Basics: getting something working
  - Advanced: making it perform

Architecture Review: Pipelines

Processor algorithm:

```
main() {
  while(true)
    do_next_instruction();
}
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Processor algorithm:

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main() {
  v
  }

do_n
  inst
  ops
  exe
  access_memory(ops, regs);
  write_back(regs);
}
```

```
main() {
  pthread_create(do_instructions);
  pthread_create(do_decode);
  pthread_create(do_execute);
  …
  pthread_join(…);
  …
}
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  …
  pthread_join(…);
  …
}
```

```
do_instructions() {
  while(true) {
    instruction = fetch();
    enqueue(DECODE, instruction);
}}
```

```
do_decode() {
  while(true) {
    instruction = dequeue();
    ops, regs = decode(instruction);
    enqueue(EX, instruction);
}}
```

```
do_execute() {
  while(true) {
    instruction = dequeue();
    execute_calc_addrs(ops, regs);
    enqueue(MEM, instruction);
}}
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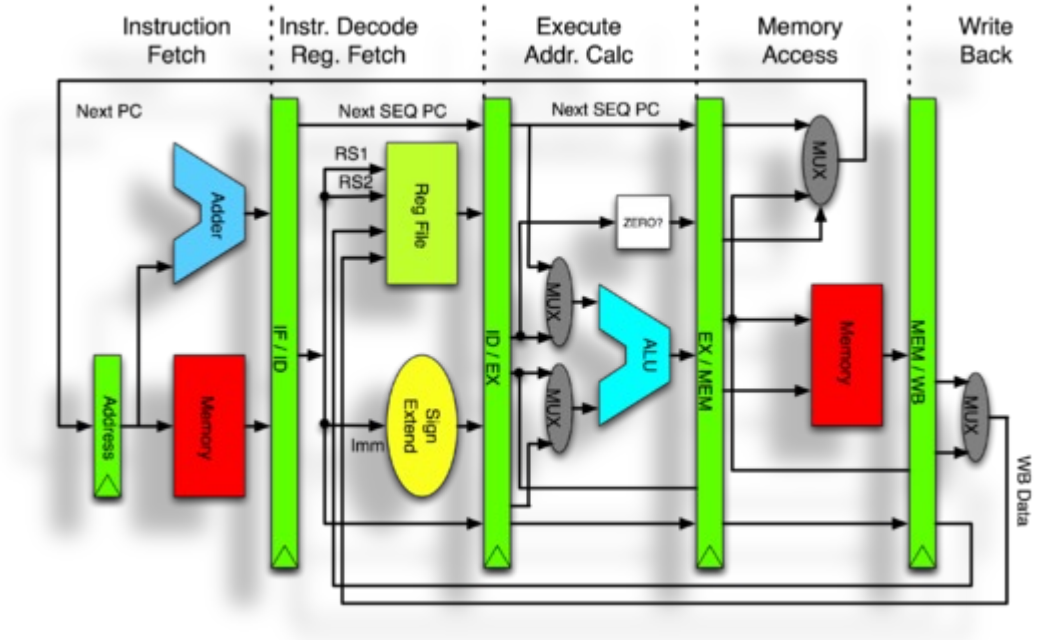


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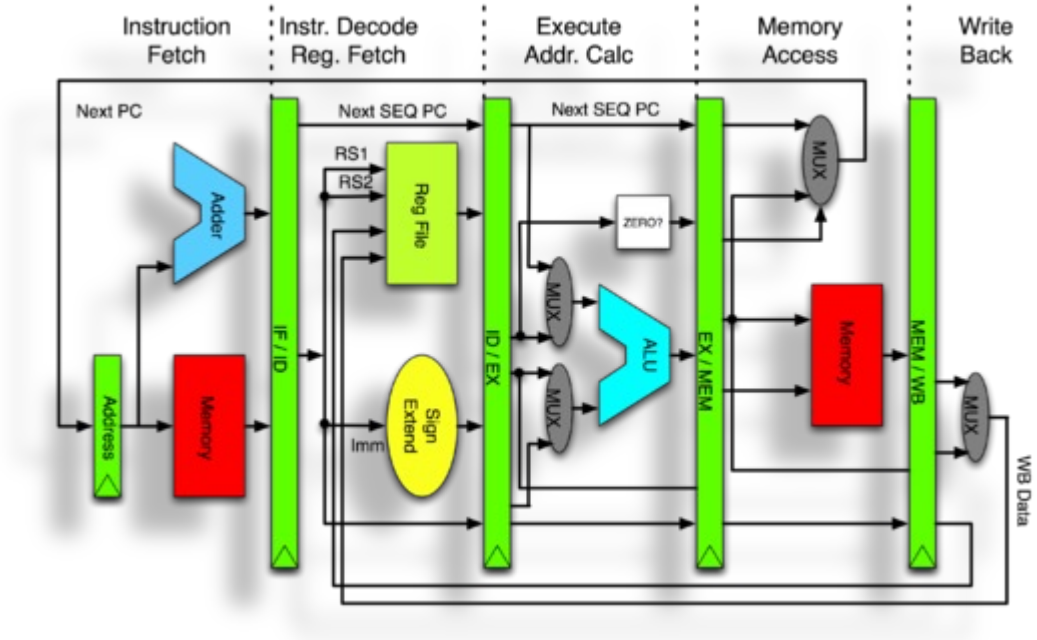


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2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

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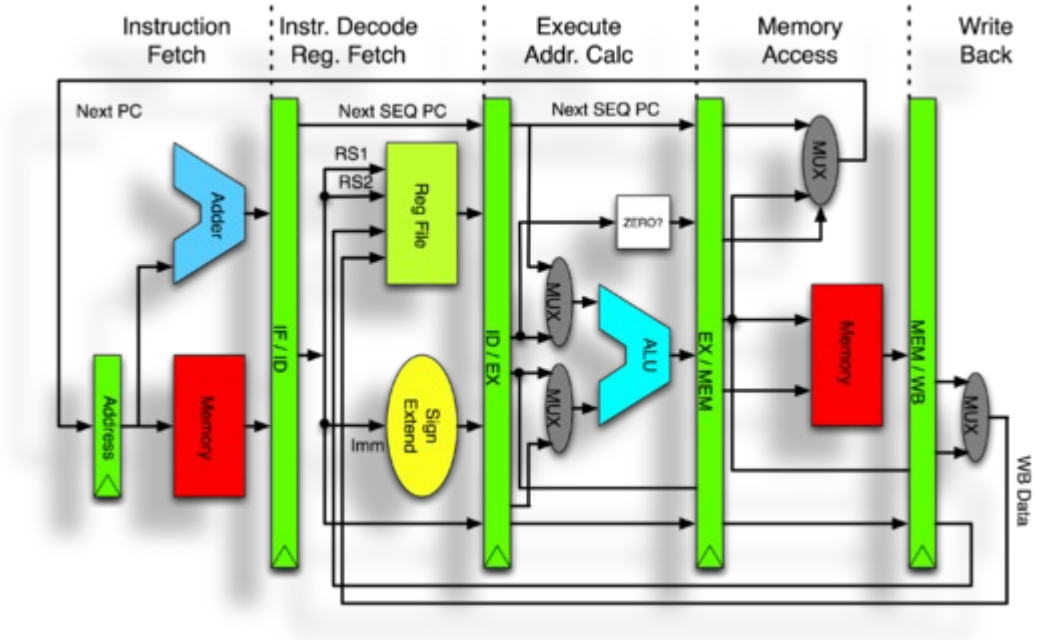


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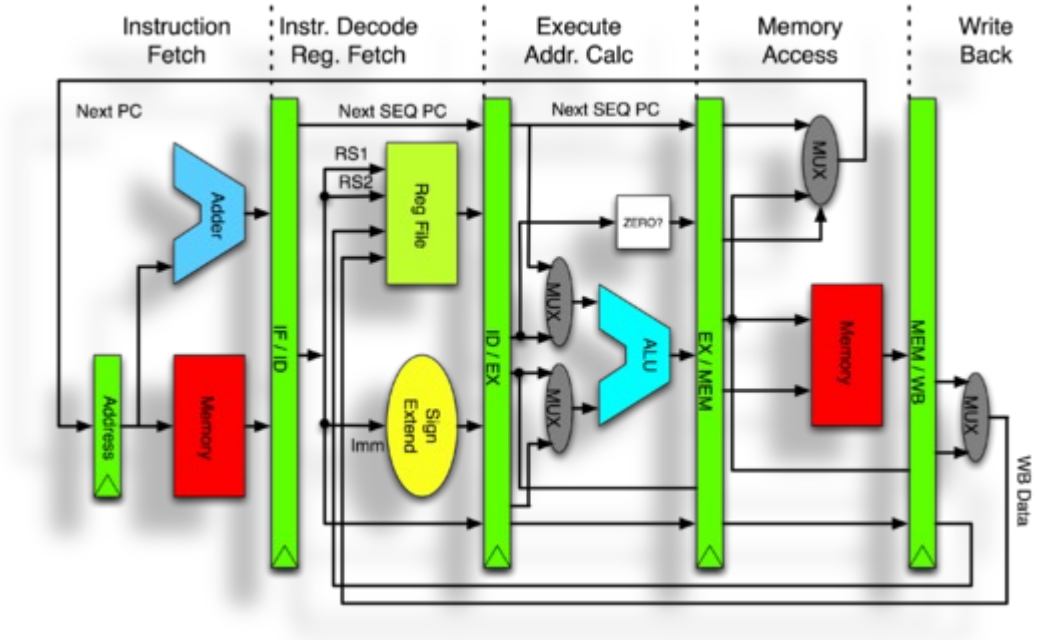


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What kinds of things cause "bubbles"/stalls?

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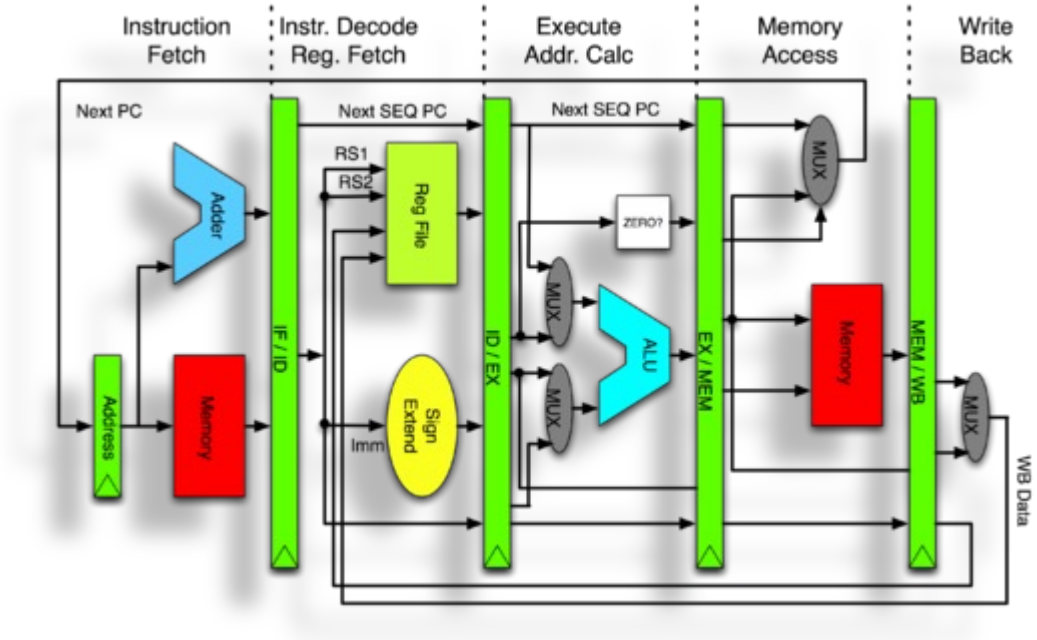


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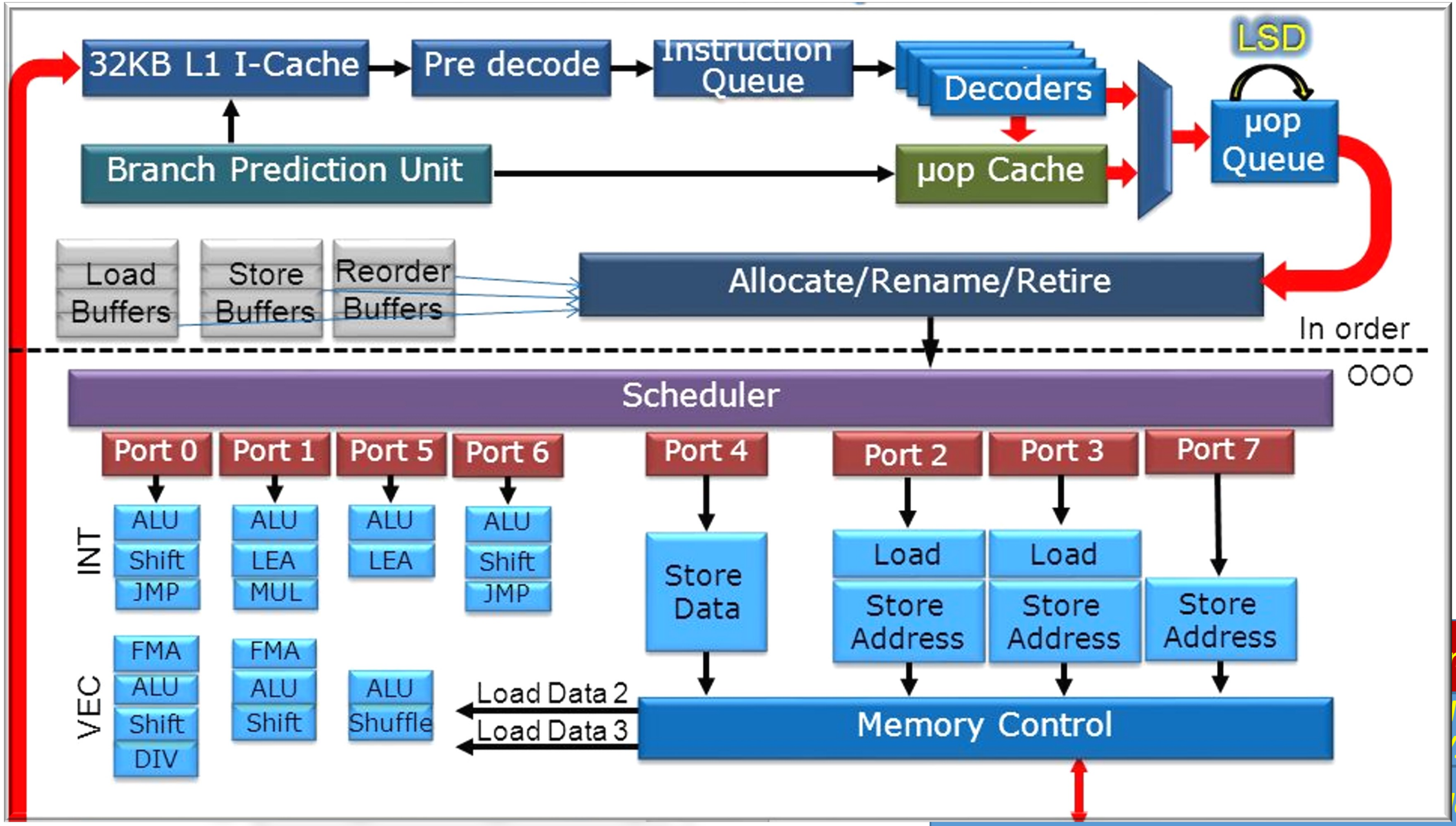
32KB L1 I-Cache
Pre decode
Instruction Queue
Decoders
LSD
µop Queue
Branch Prediction Unit
µop Cache
Load Buffers
Store Buffers
Reorder Buffers
Allocate/Rename/Retire
In order
OOO
Scheduler
Port 0
Port 1
Port 5
Port 6
Port 4
Port 2
Port 3
Port 7
INT
ALU
Shift
JMP
ALU
LEA
MUL
ALU
LEA
ALU
Shift
JMP
VEC
FMA
ALU
Shift
DIV
FMA
ALU
Shift
ALU
Shuffle
Store Data
Load
Store Address
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Load Data 2
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Memory Control

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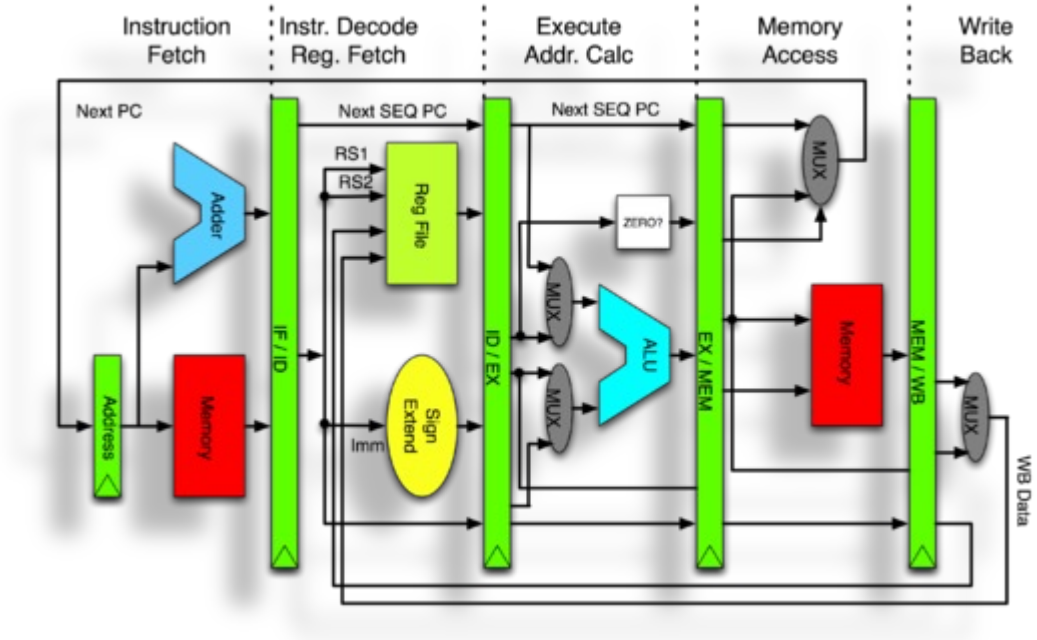


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Multi-core/SMPs

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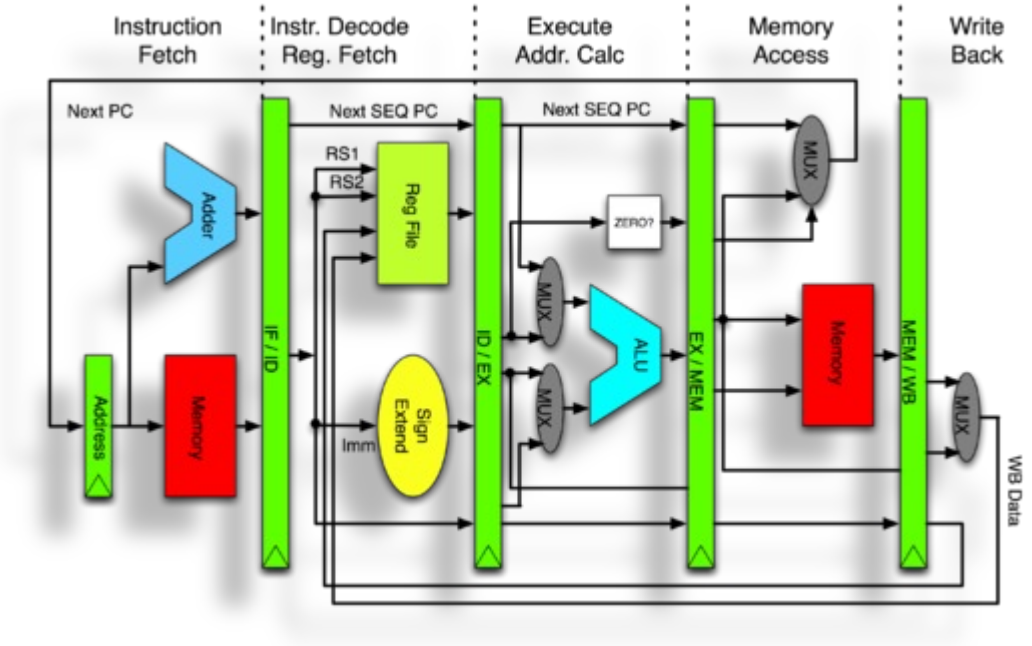

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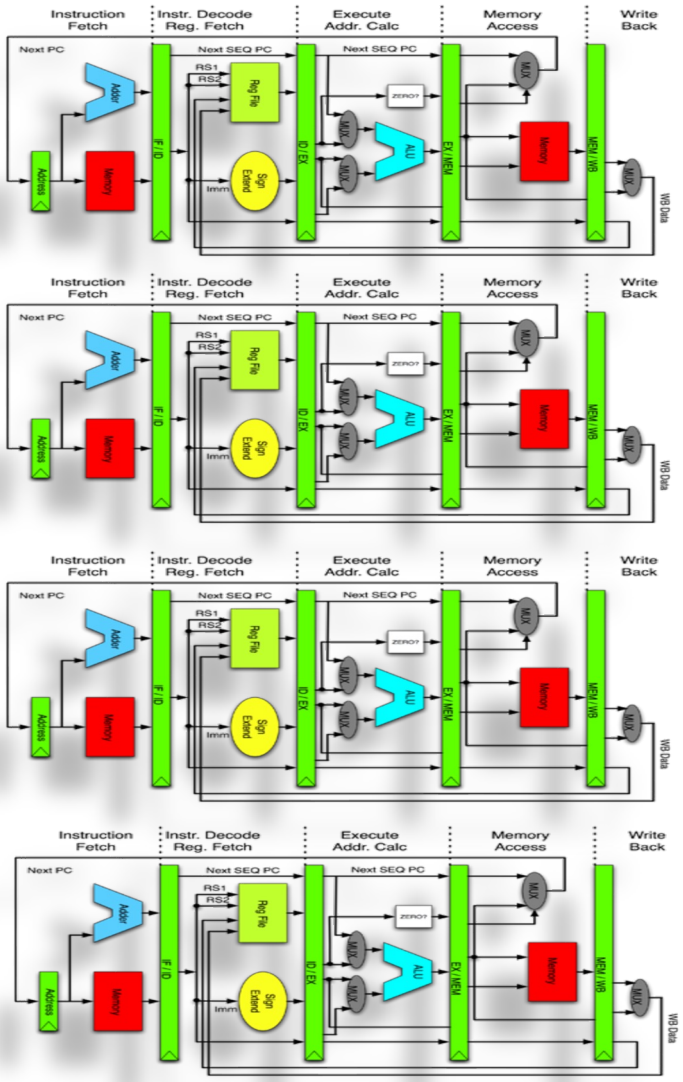

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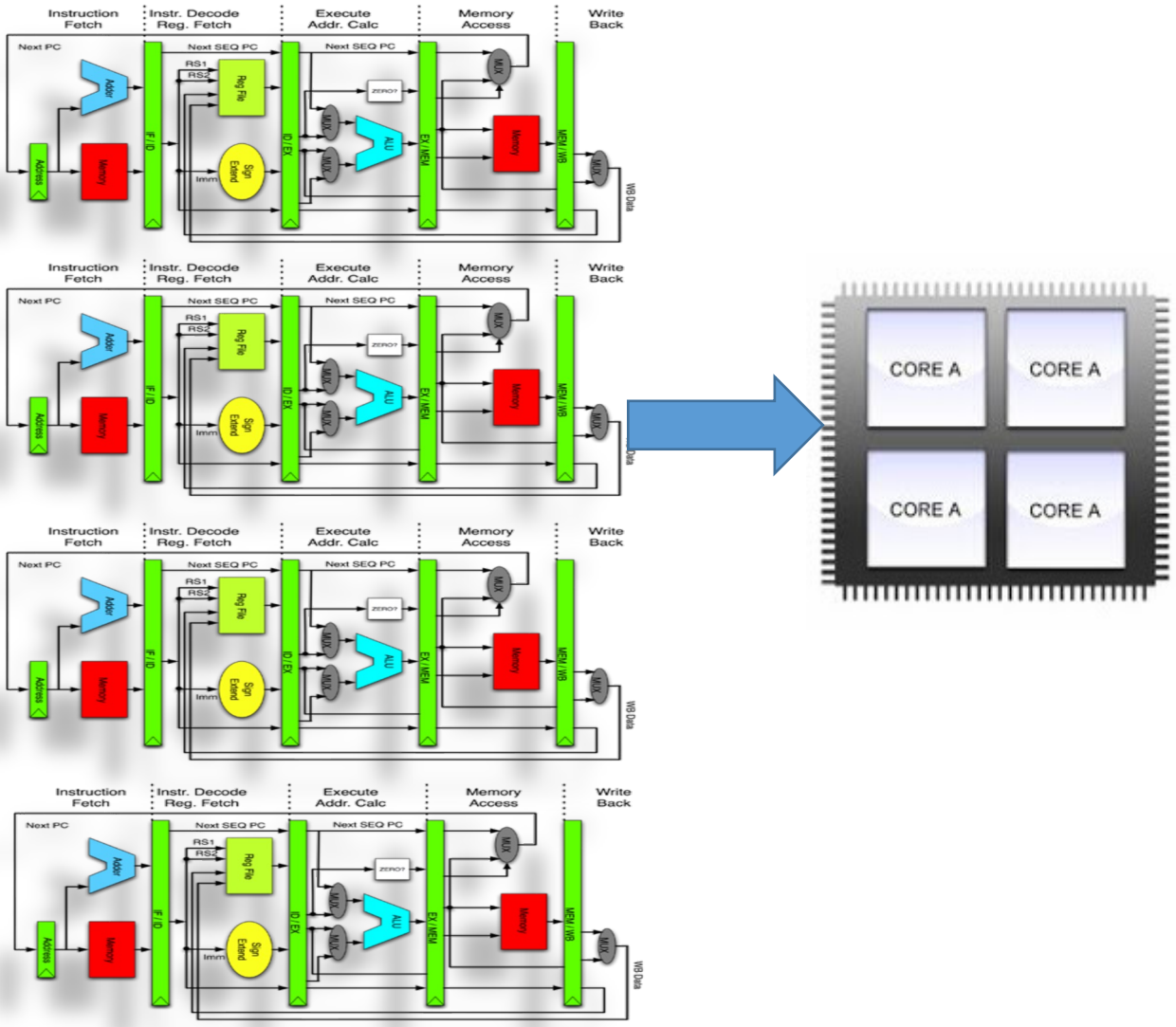

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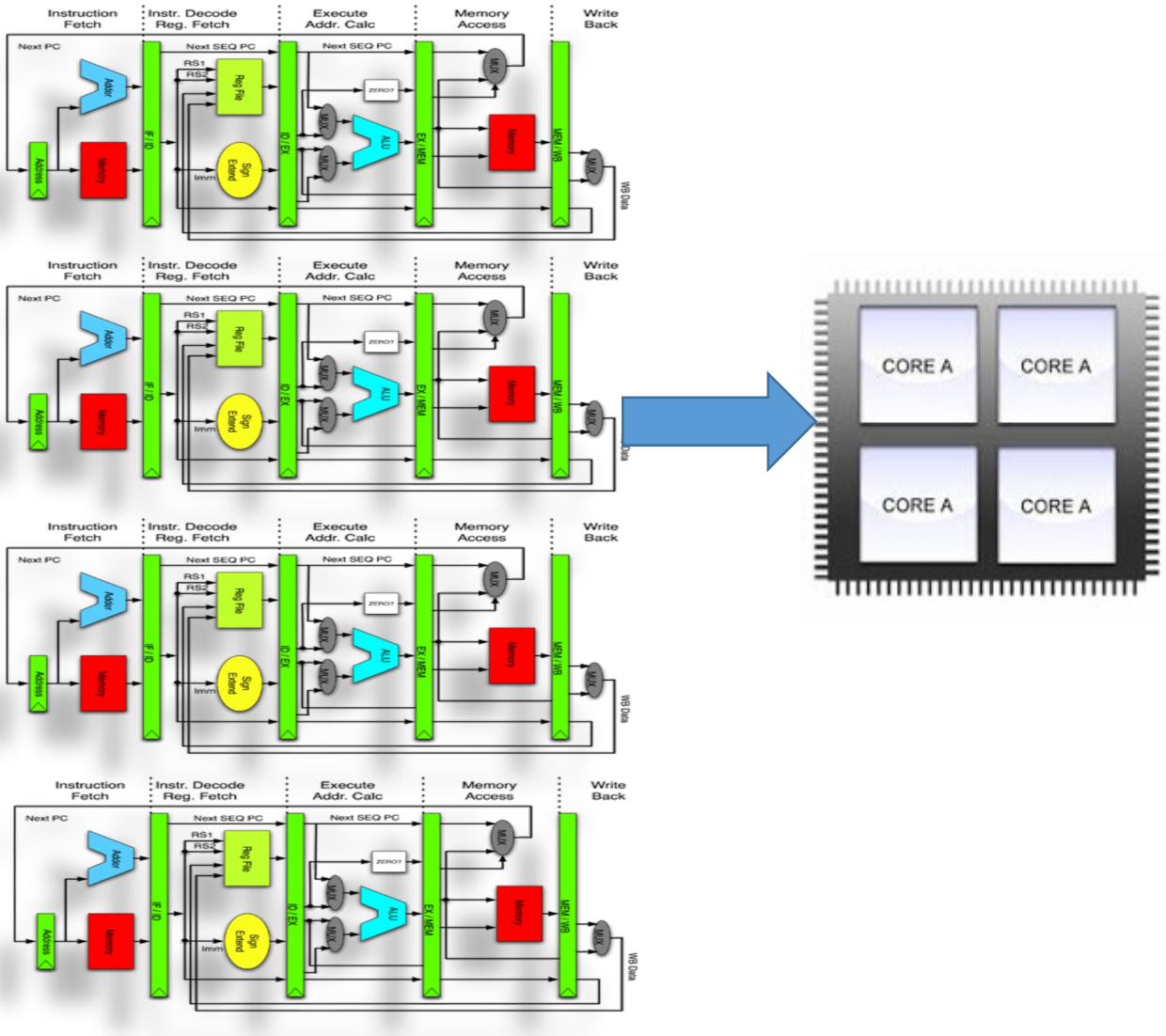


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  }
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- ***Pros: Simple***
- ***Cons: programmer has to find the parallelism!***

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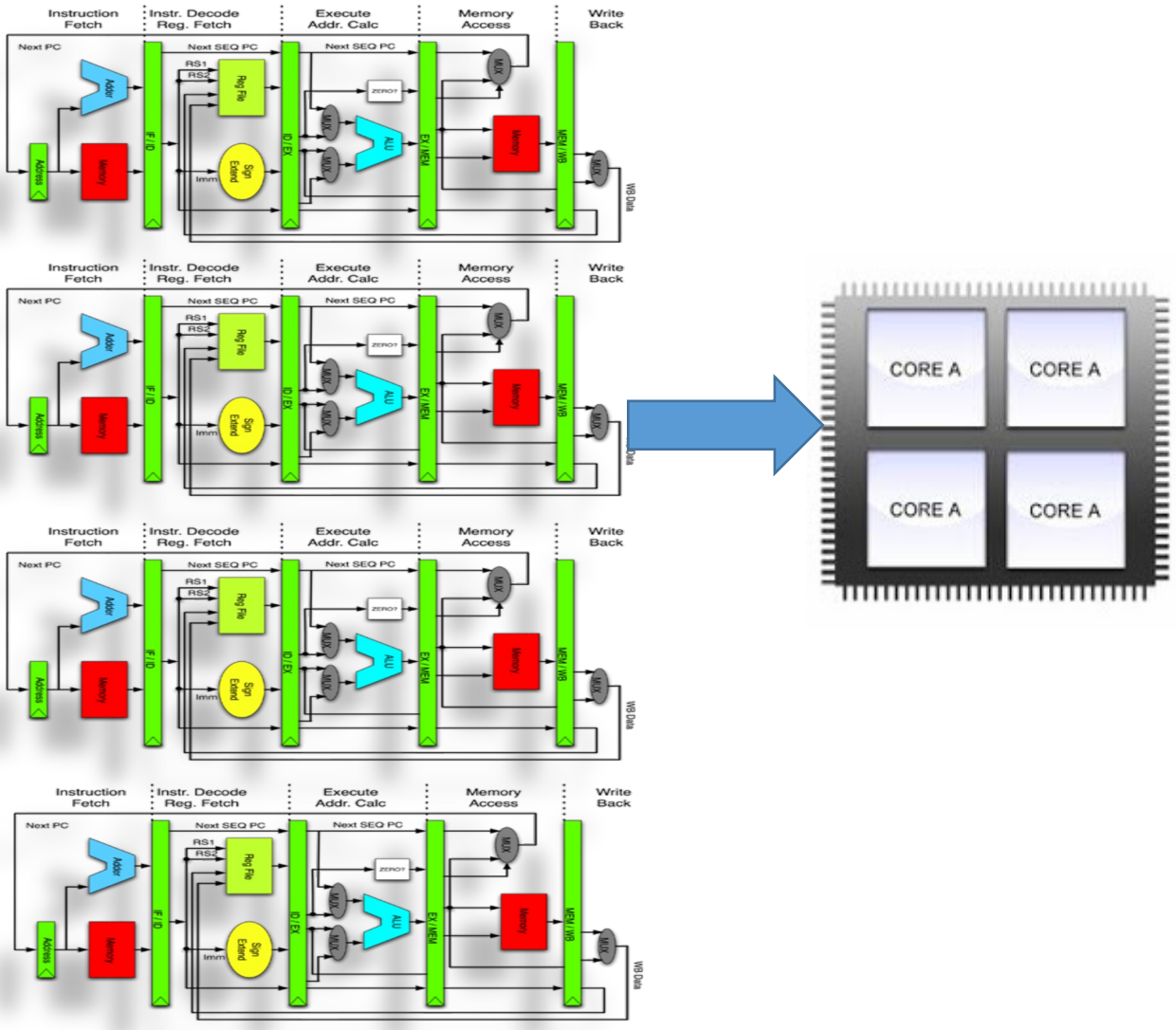


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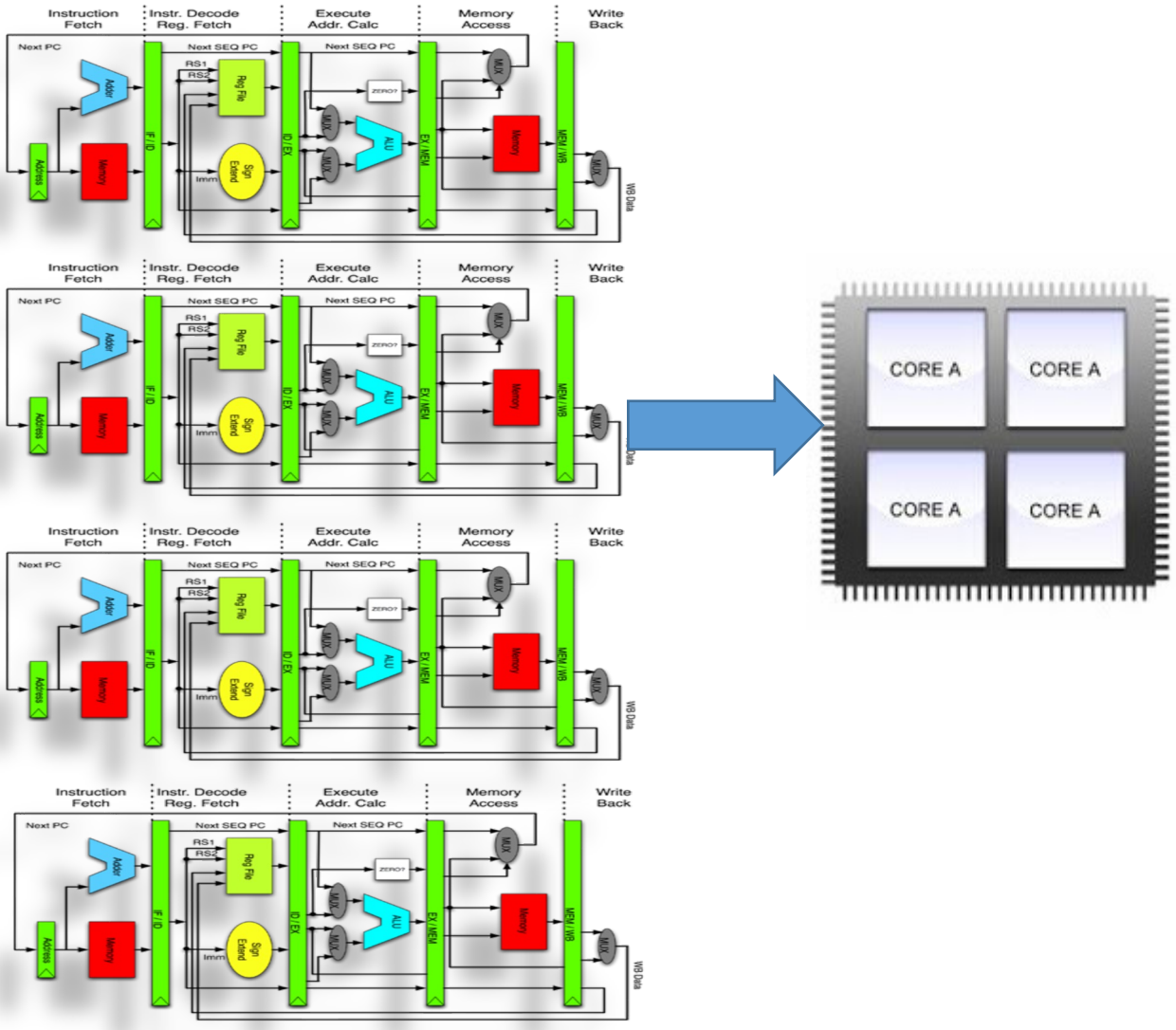


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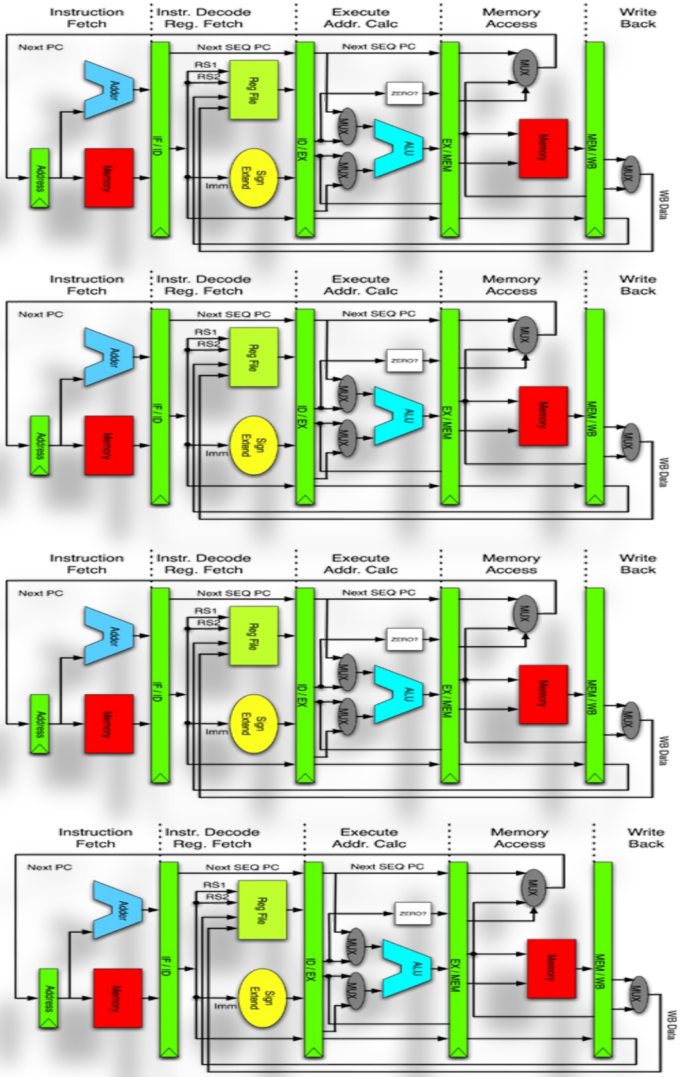
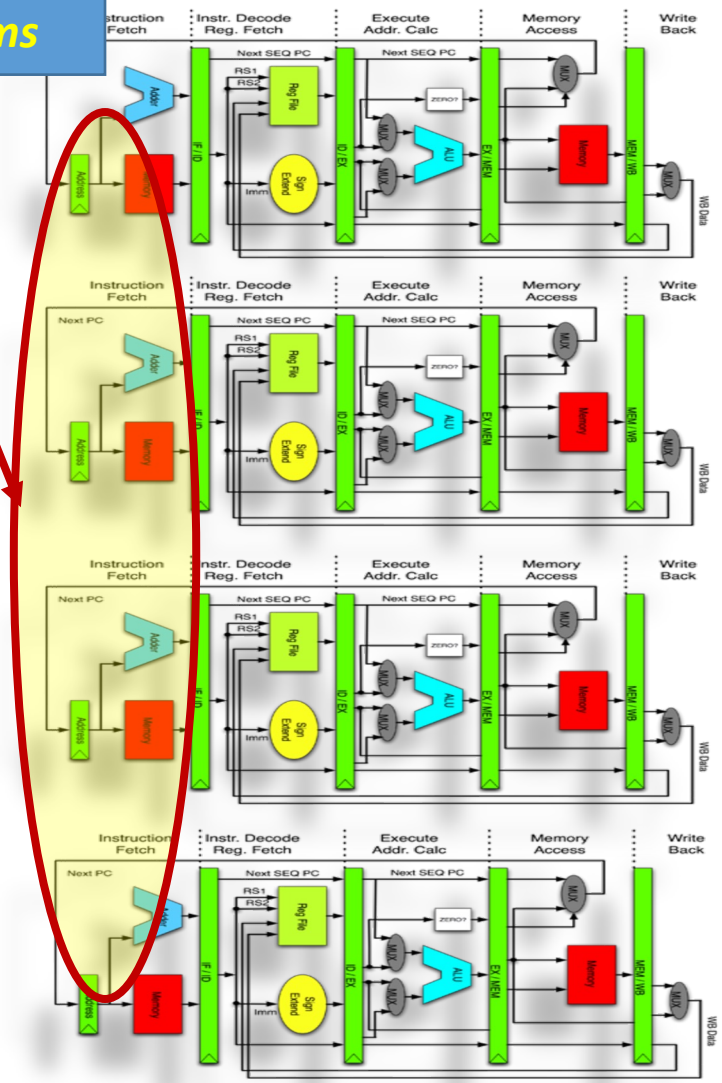
Other techniques extract parallelism here, try to let the machine find parallelism

Superscalar processors



Superscalar processors

Remove extra instruction streams



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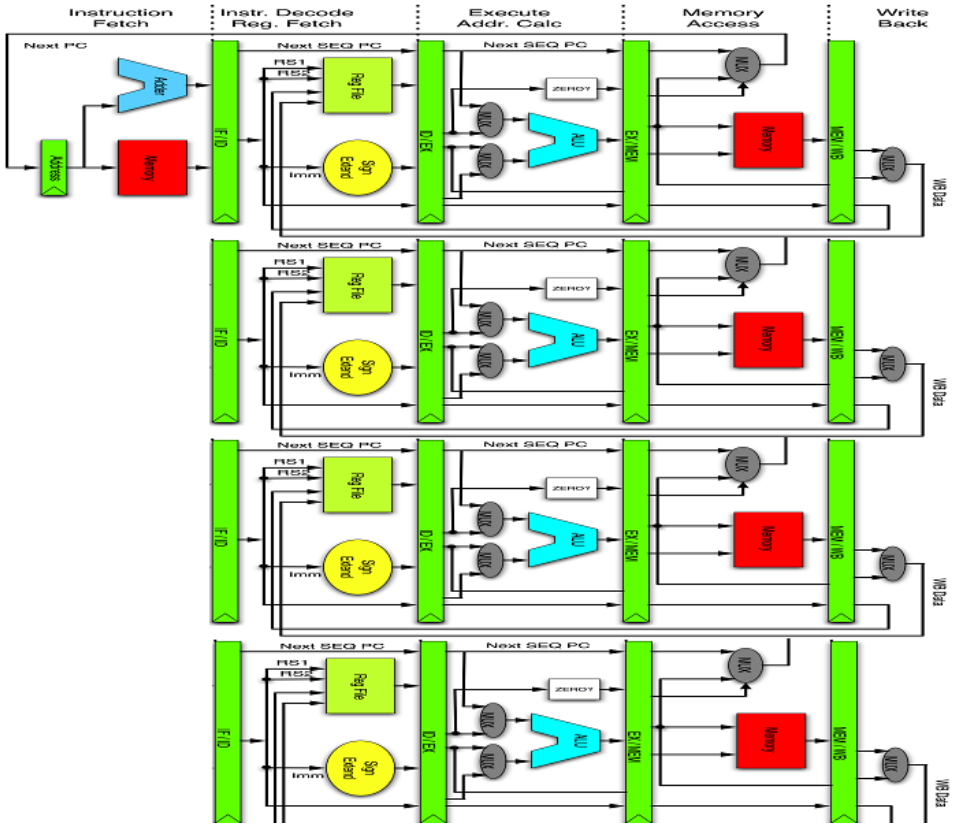

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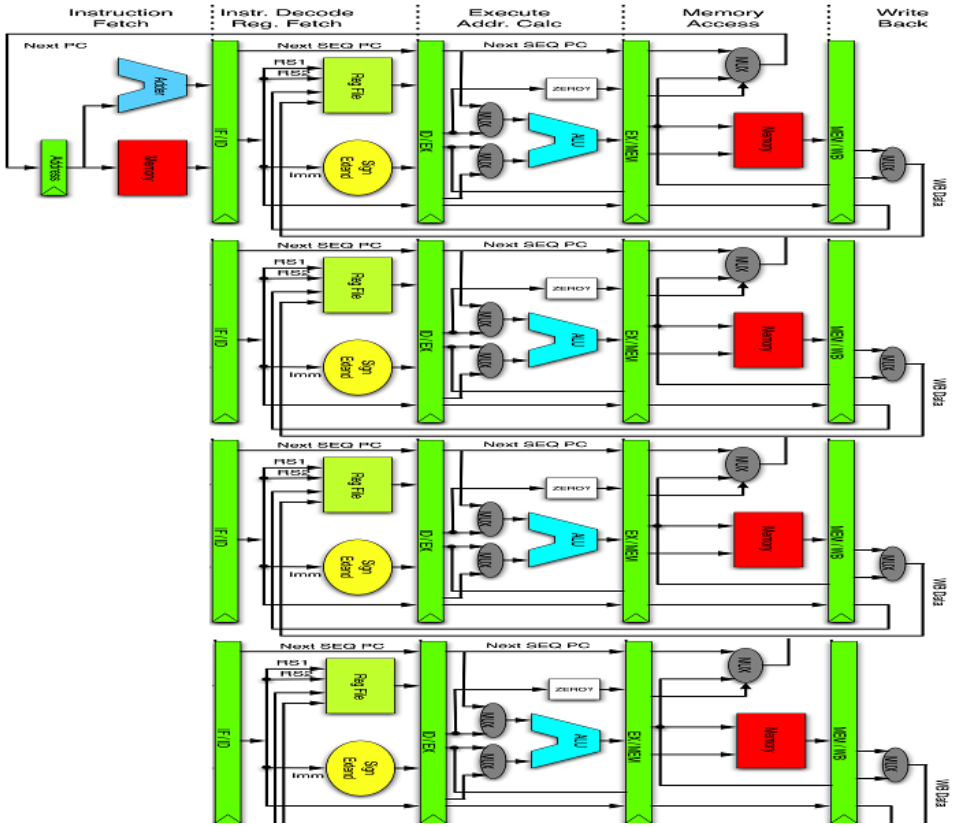


```
main() {
  for(i=0; i<CORES; i++)
    pthread_create(decode_exec);
    while(true) {
      instruction = fetch();
      enqueue(instruction);
    }
}

decode_exec() {
  instruction = dequeue();
  ops, regs = decode(instruction);
  execute_calc_addrs(ops, regs);
  access_memory(ops, regs);
  write_back(regs);
}
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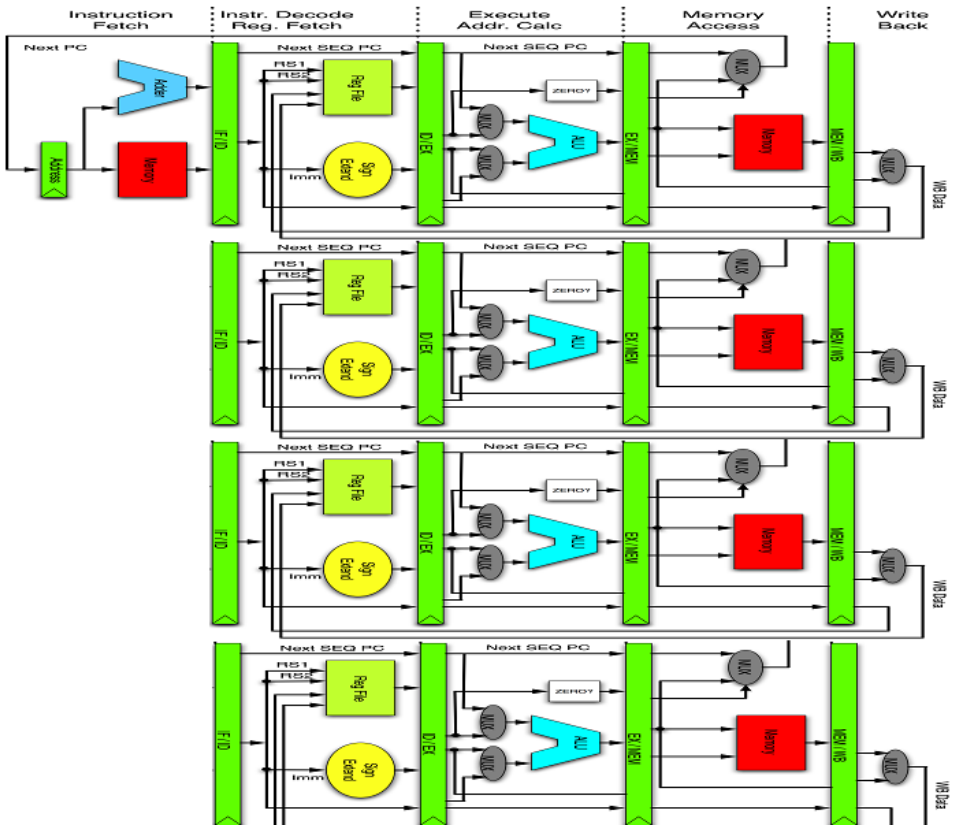
Superscalar processors

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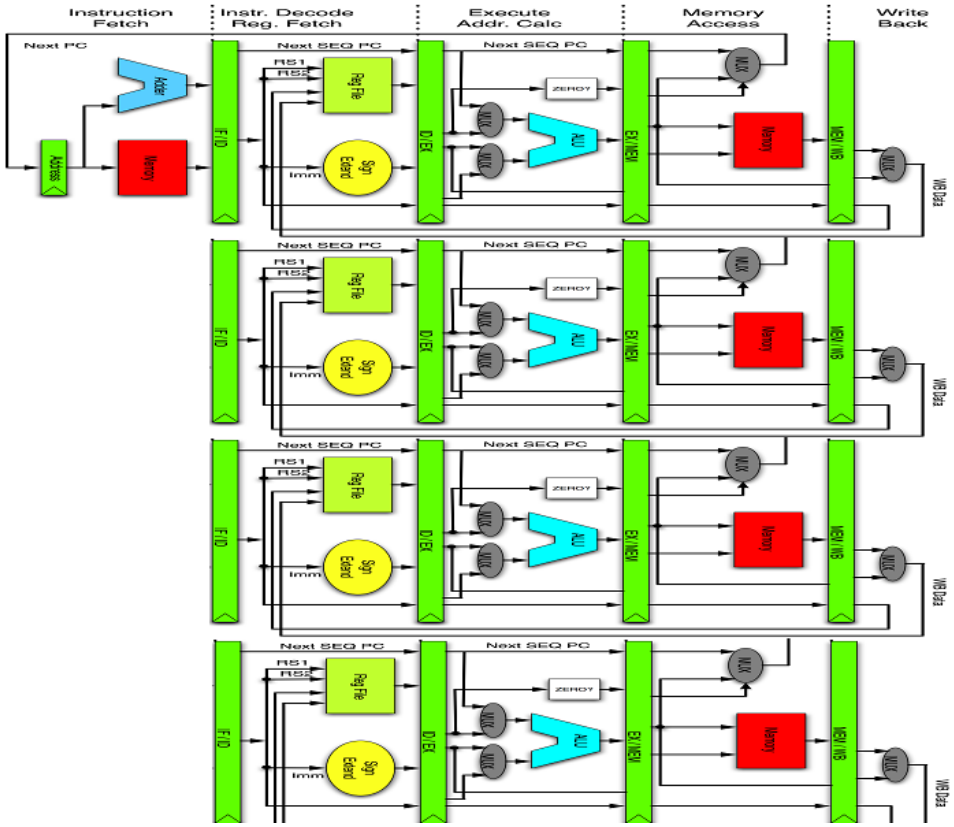


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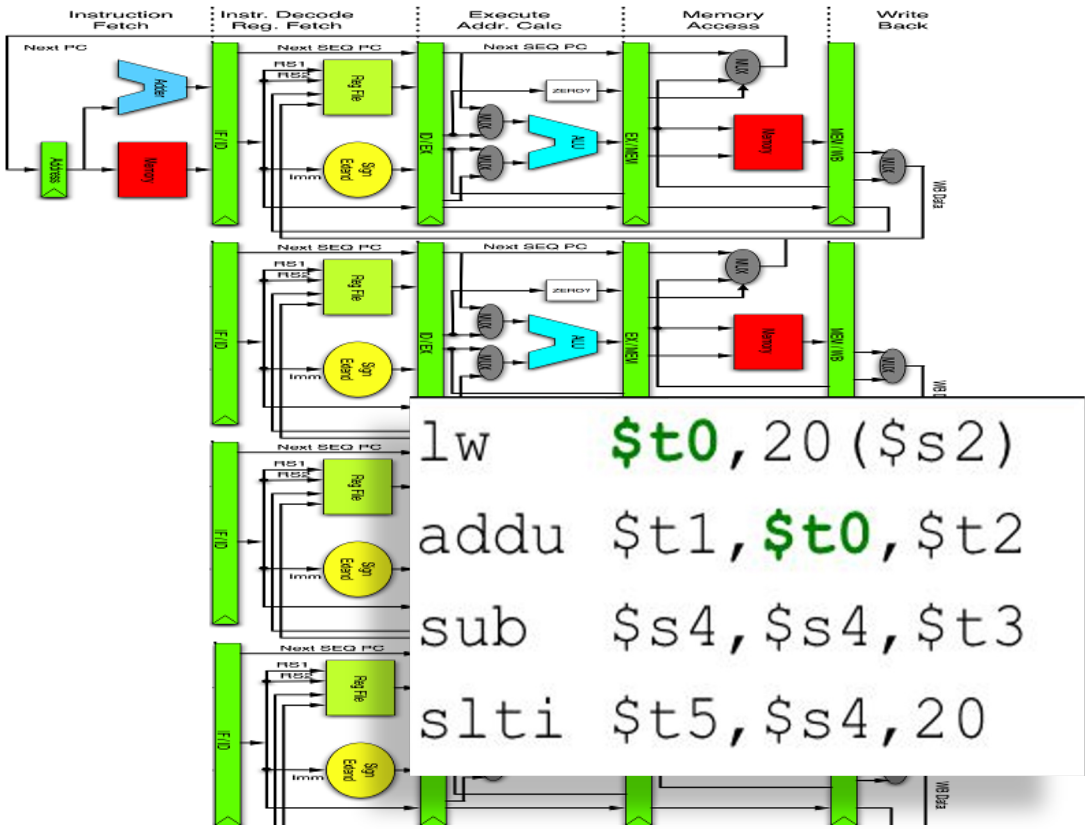
Enables independent instruction parallelism.

Superscalar processors

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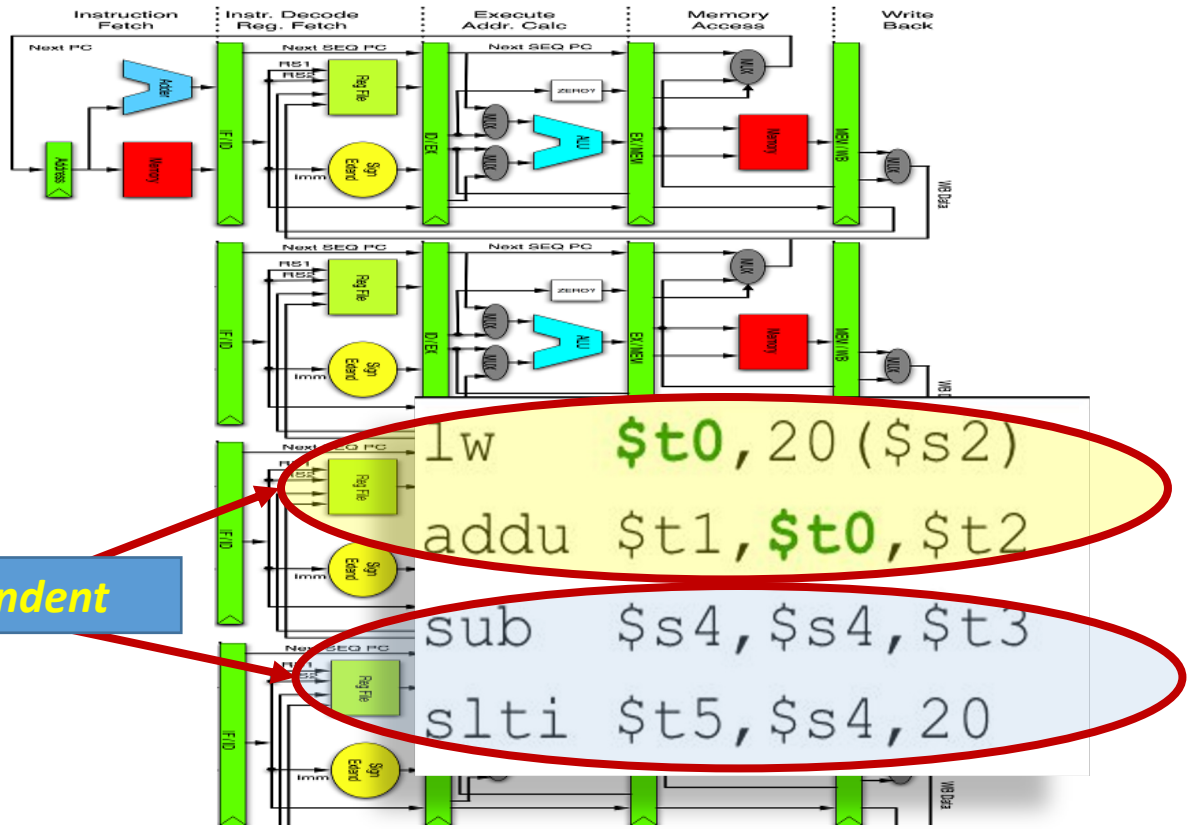
    while(true) {
      instruction = fetch();
      enqueue(instruction);
    }
}

decode_exec() {
  instruction = dequeue();
  ops, regs = decode(instruction);
  execute_calc_addrs(ops, regs);
  access_memory(ops, regs);
  write_back(regs);
}
```

Doesn't look that different does it? Why do it?

Enables independent instruction parallelism.

Superscalar processors



independent

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Vector/SIMD processors

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   L.D    F0, 0(R1)
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   ADD.D  F4, F2, F0
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   DSUBIU R4, 1
   BNEZ   R4, loop
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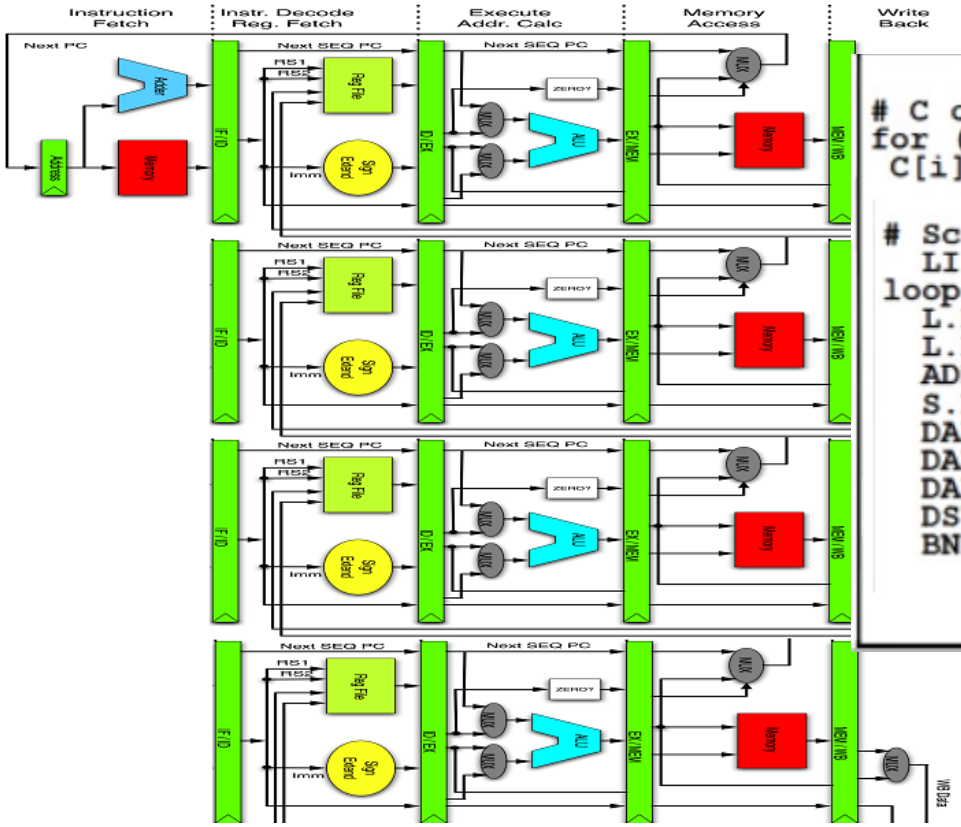
Vector/SIMD processors

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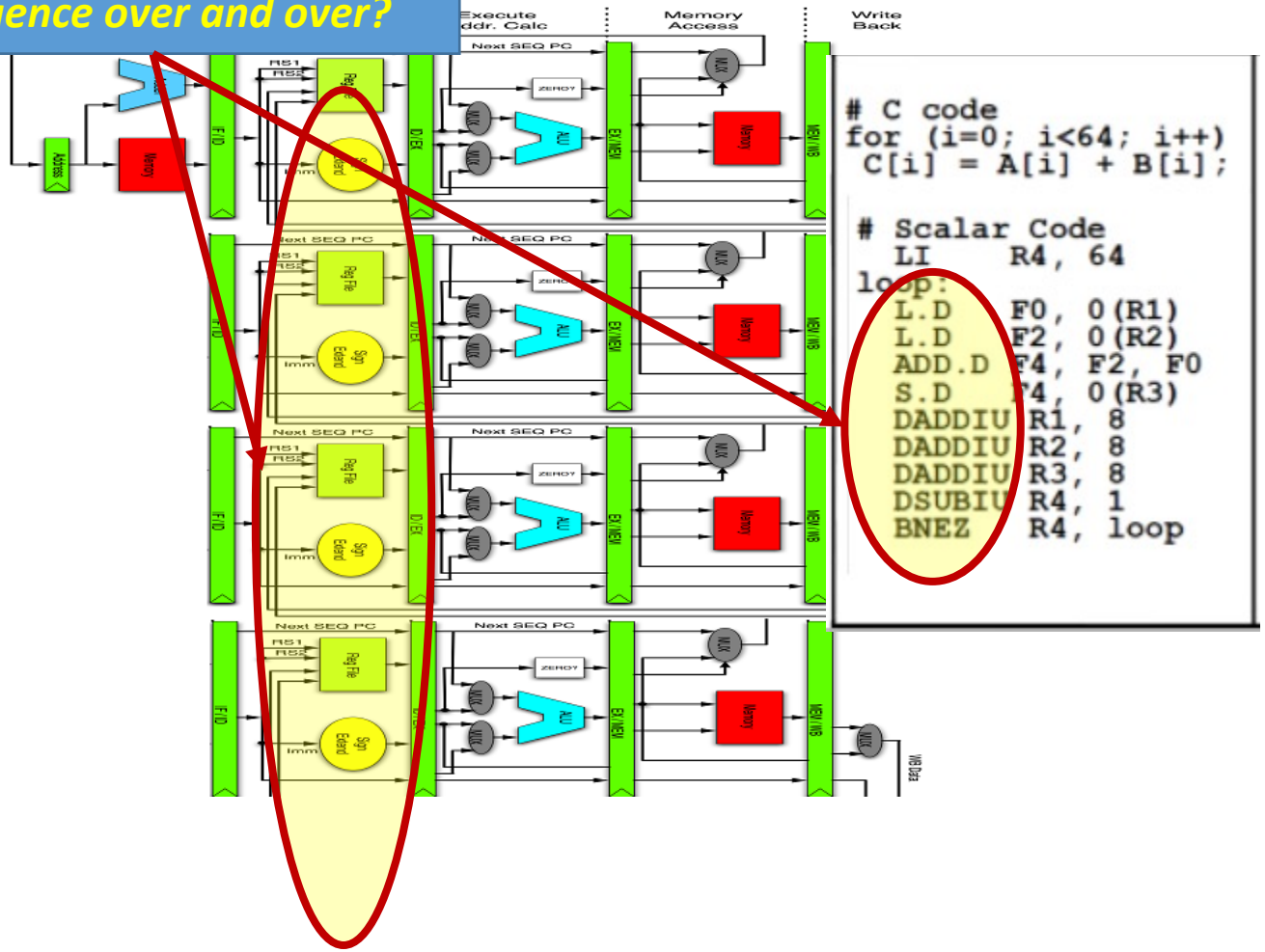
Vector/SIMD processors

Why decode same instruction sequence over and over?

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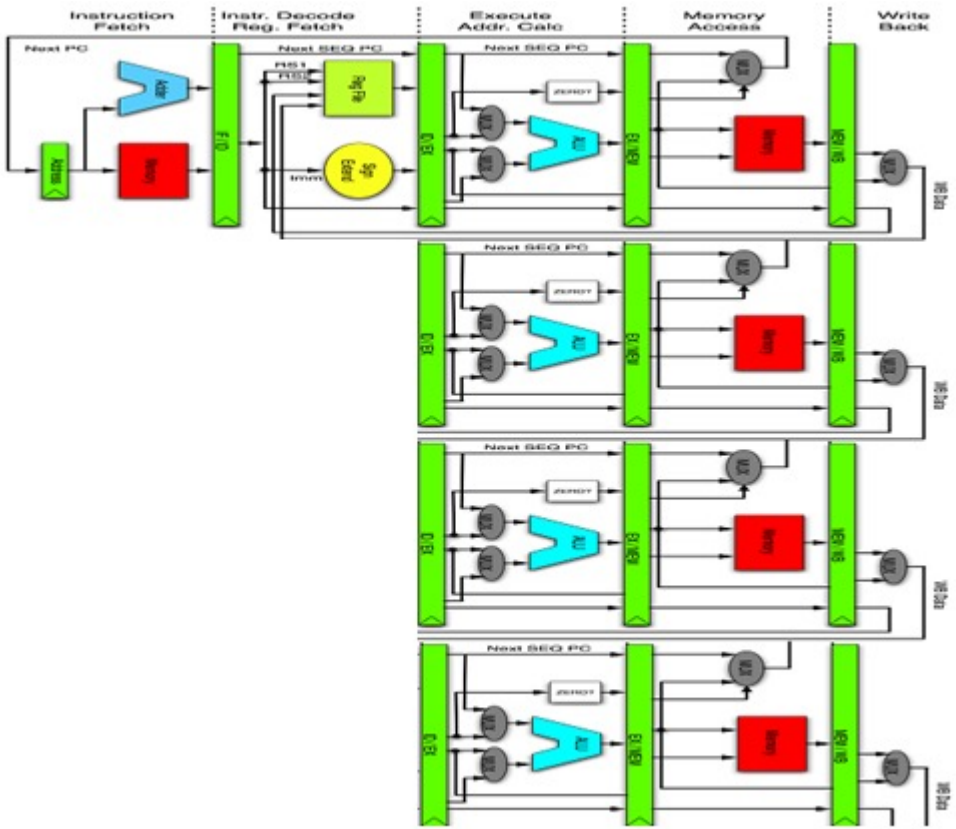

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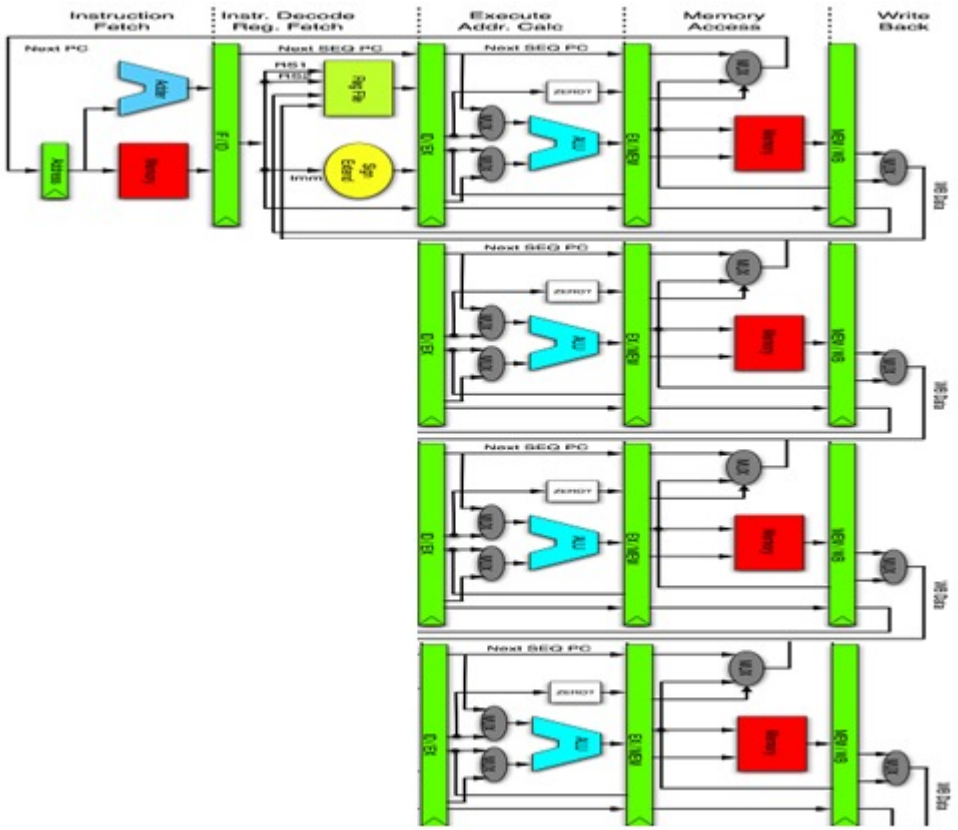


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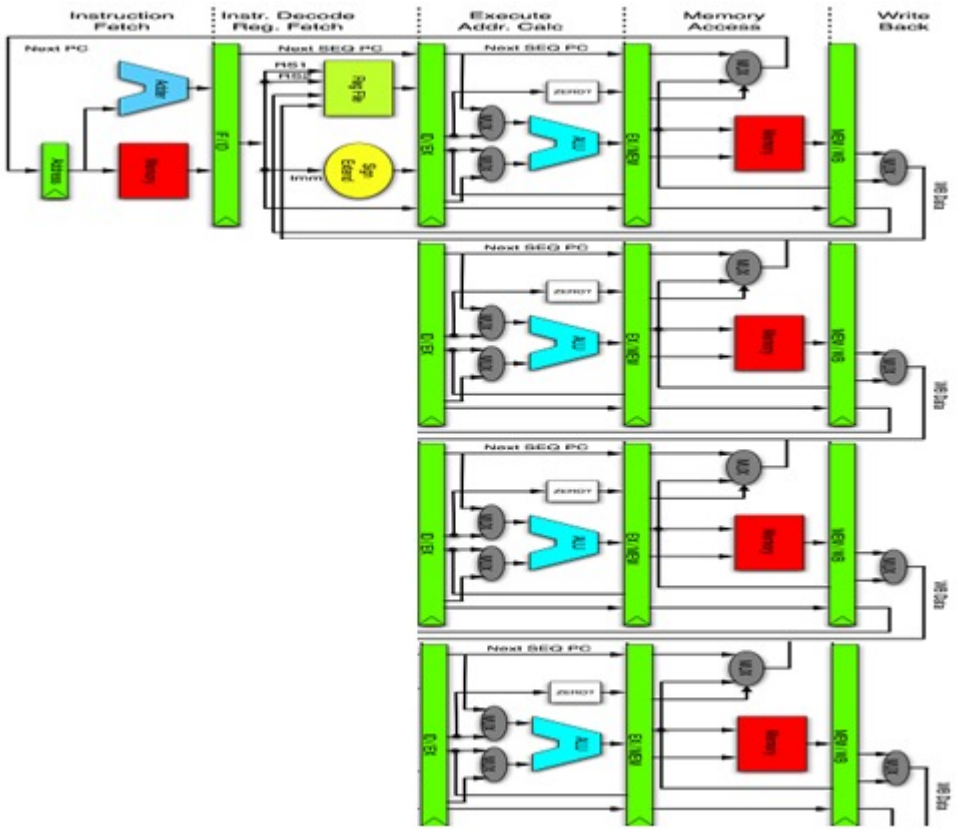
Vector/SIMD processors

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Single instruction stream, multiple computations

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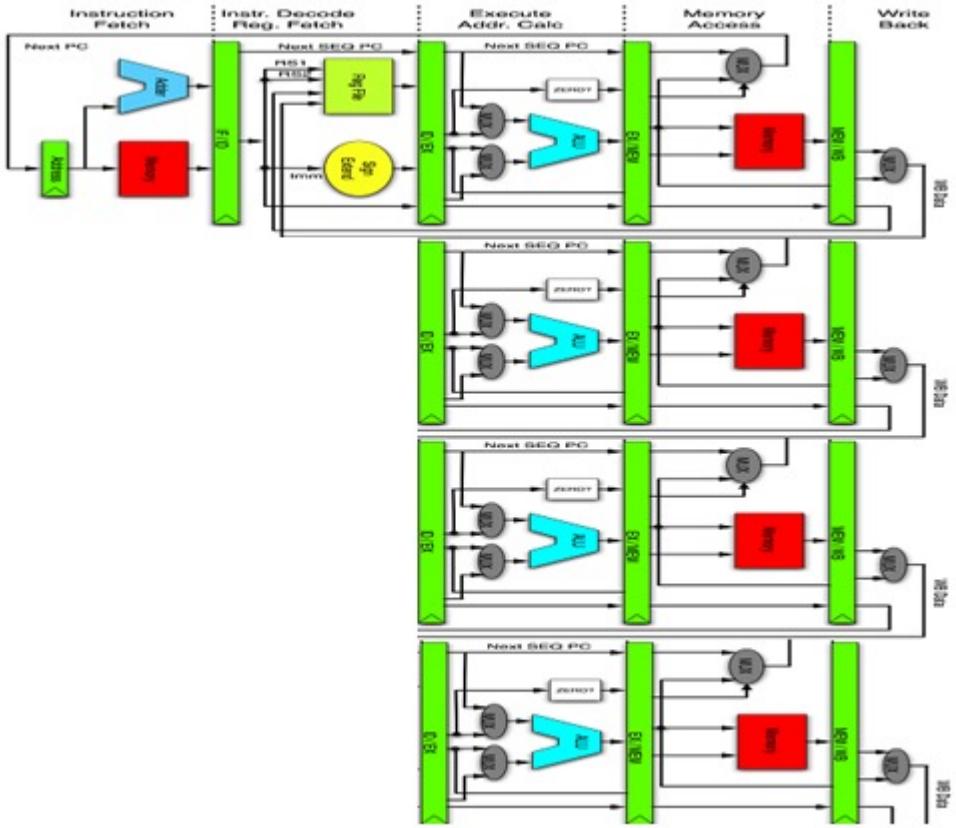


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Single instruction stream, multiple computations

But now all my instructions need multiple operands!

Vector Processors

- Process multiple data elements simultaneously.
- Common in supercomputers of the 1970’s 80’s and 90’s.
- Modern CPUs support some vector processing instructions
  - Usually called SIMD
- Can operate on a few vectors elements per clock cycle in a pipeline or,
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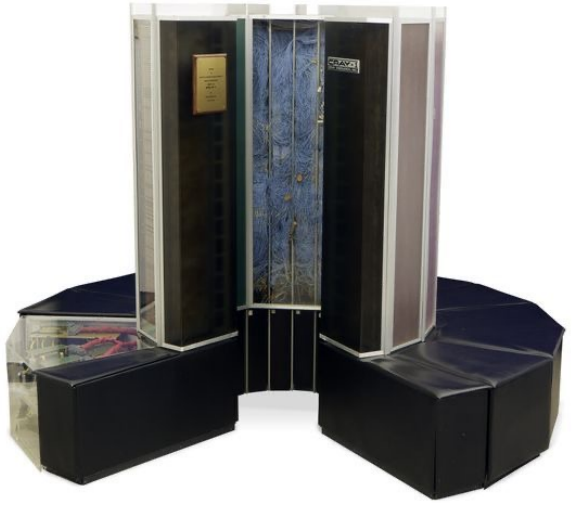
Vector Processors



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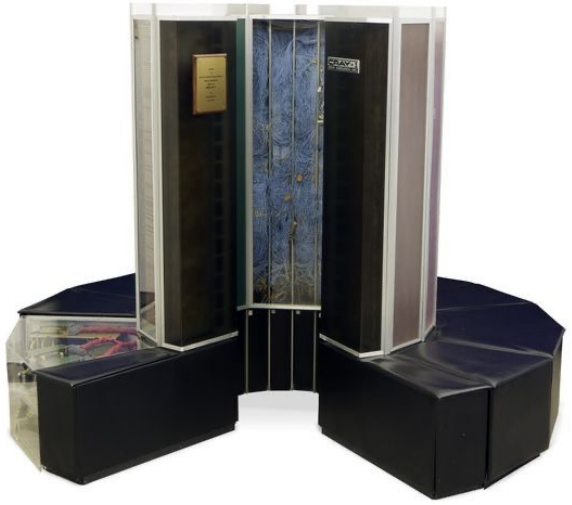
Vector Processors



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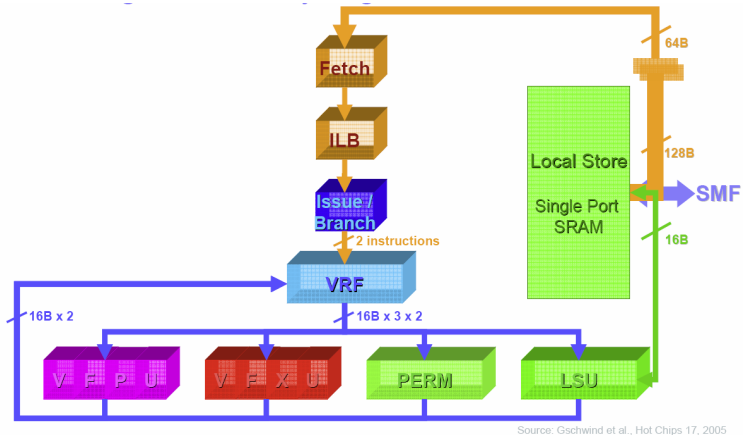
Single instruction stream, multiple data → Programming model has to change

Vector Processors



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- Same instruction stream executed on
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- Multiple different operands in parallel

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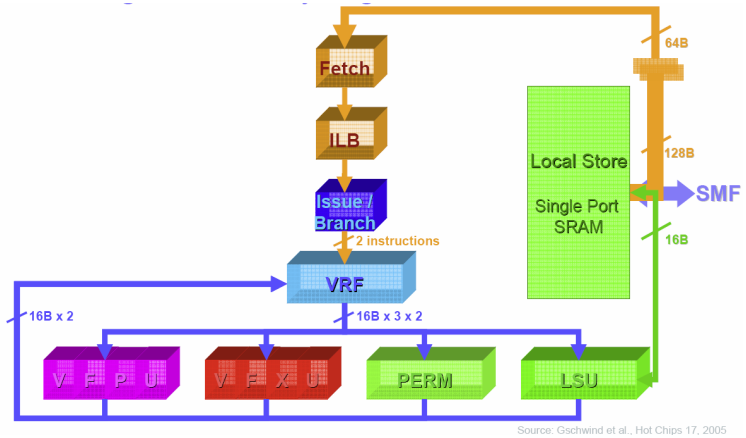

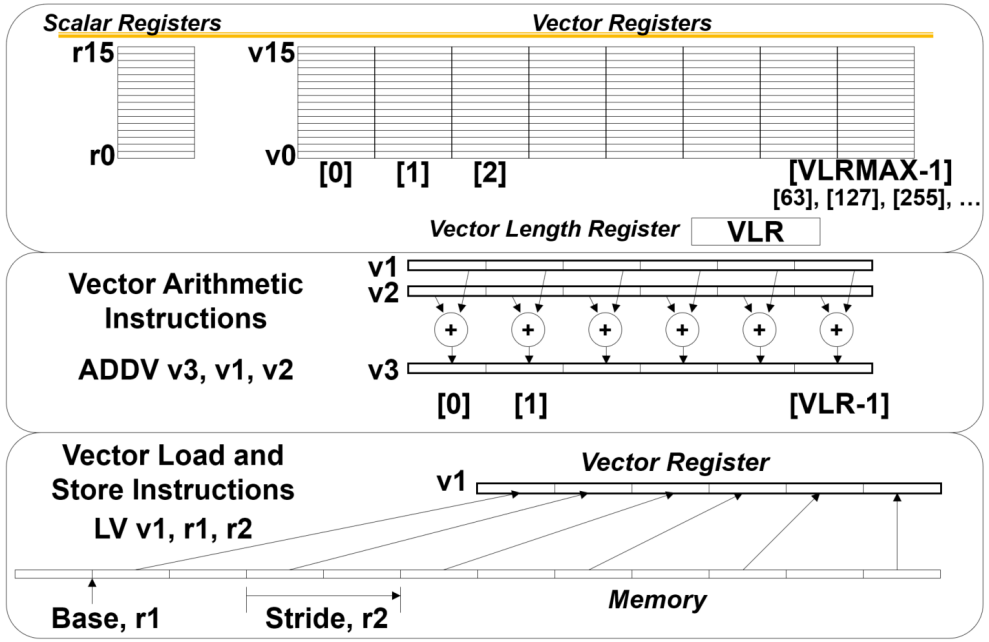

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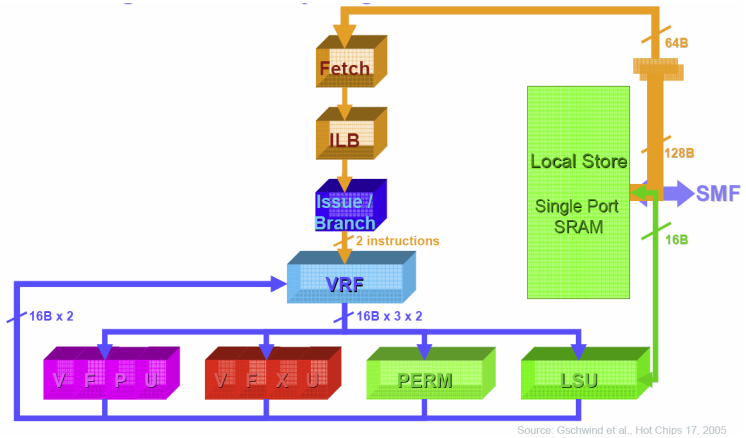

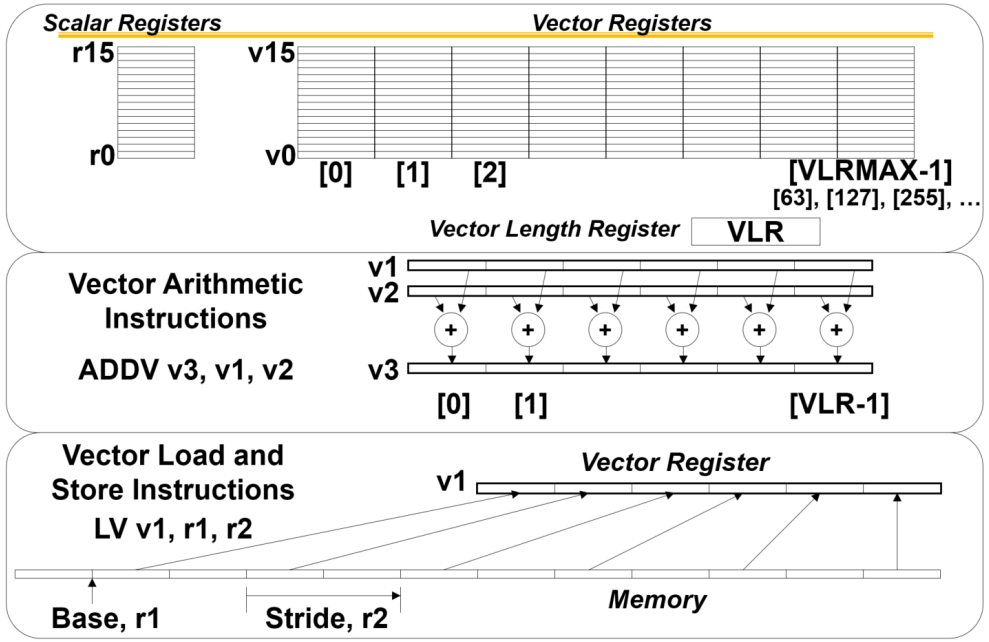

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```
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   LI     VLR, 64
   LV     V1, R1
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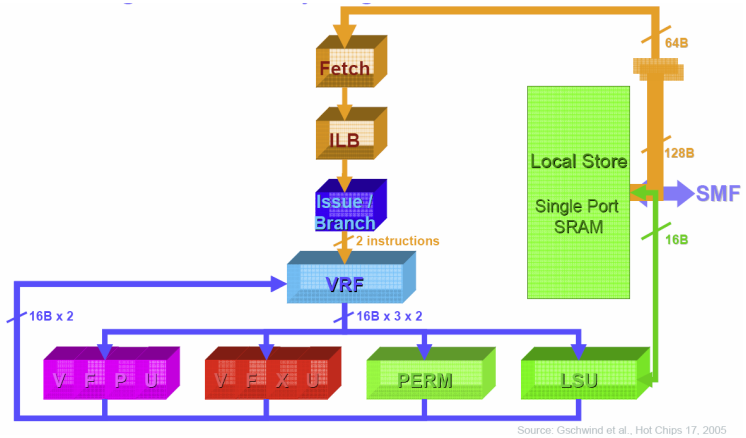
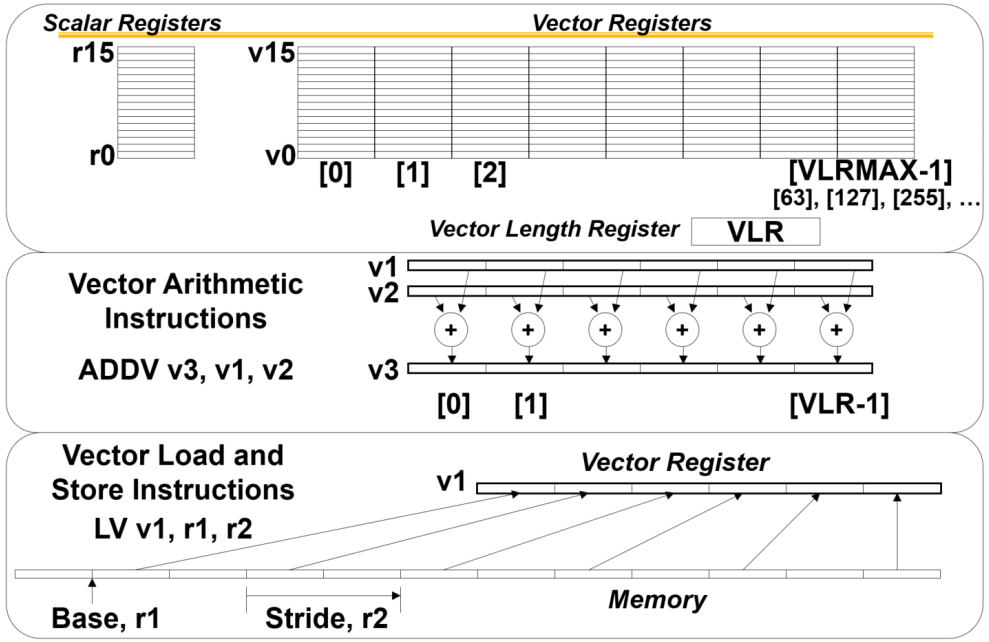
   ADDV.D V3, V1, V2
   SV     V3, R3
```

Vector Processors

GPUs: same basic idea





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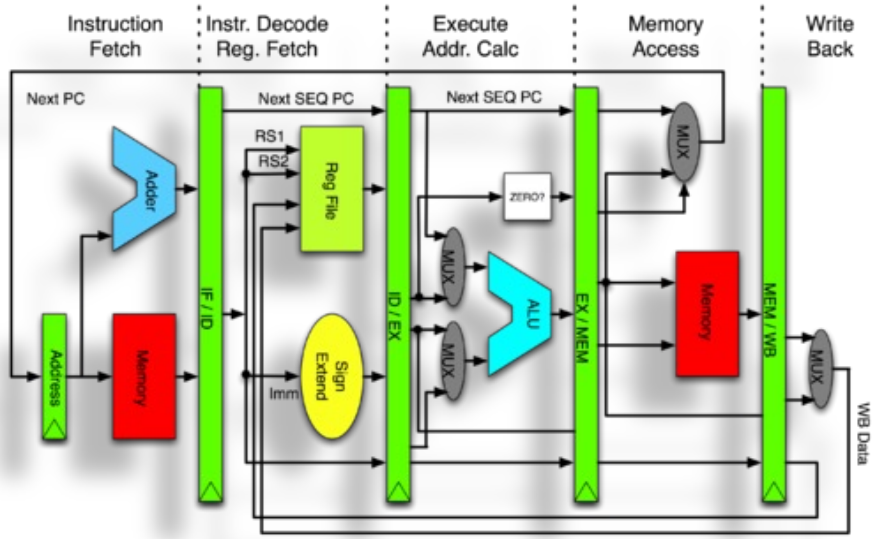
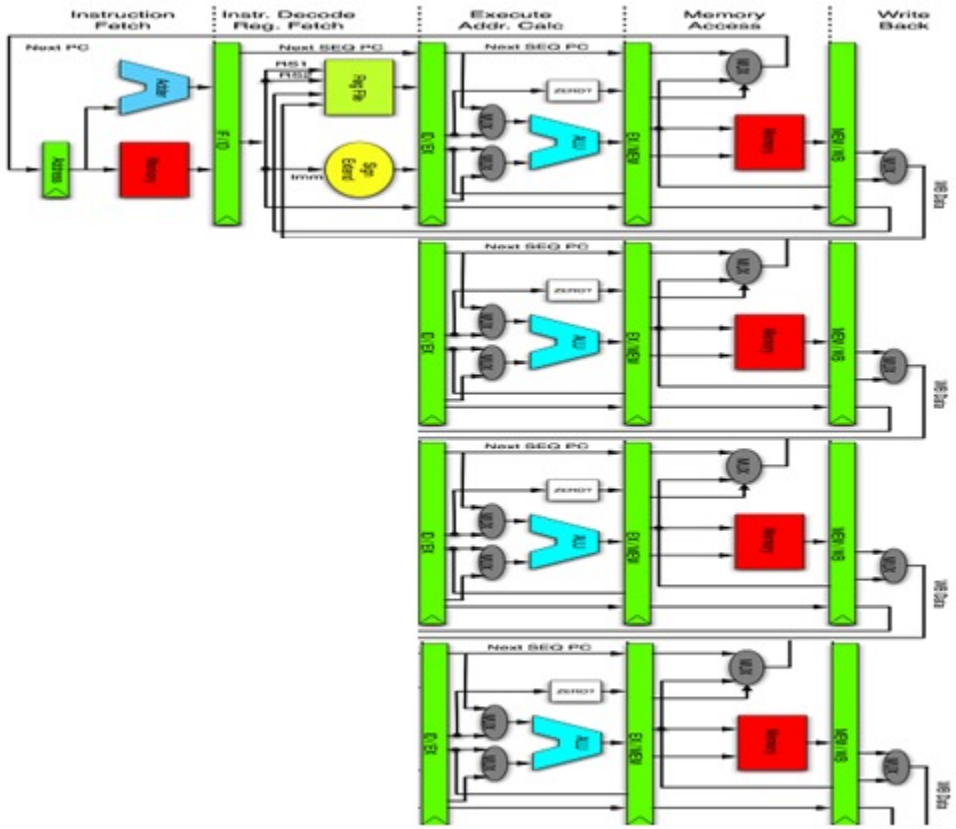
When does vector processing help?





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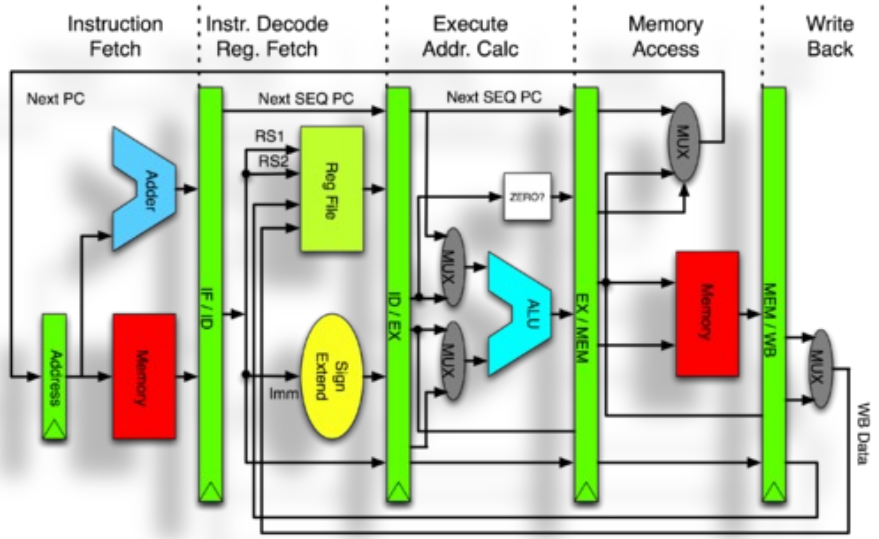
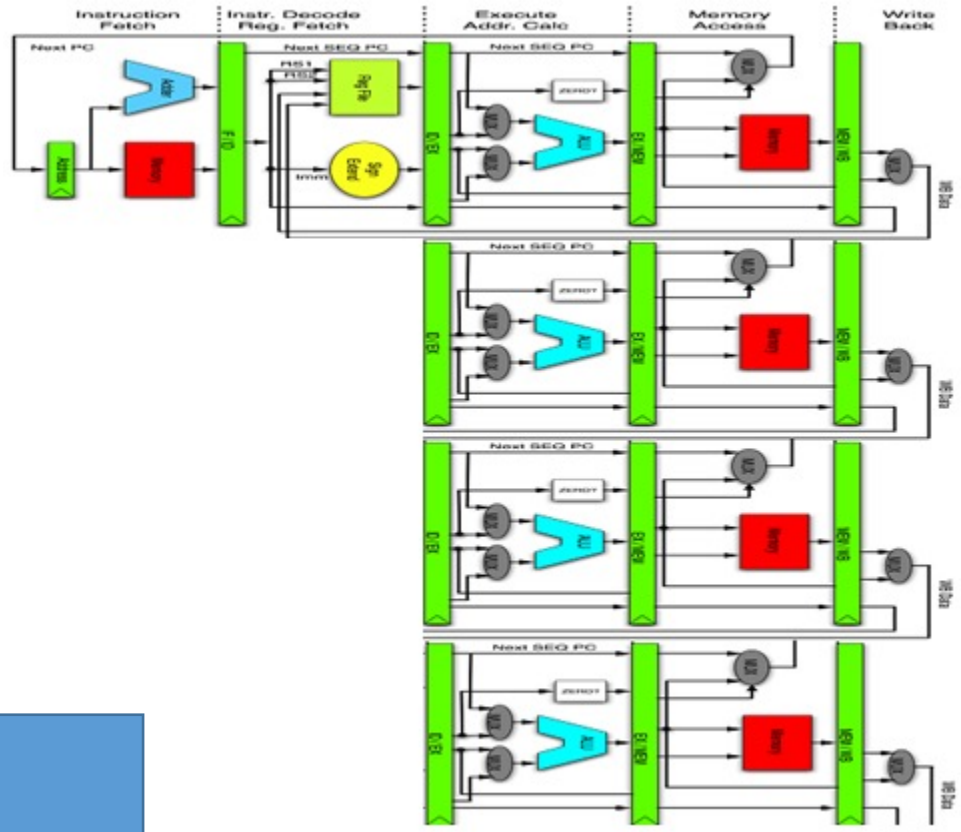
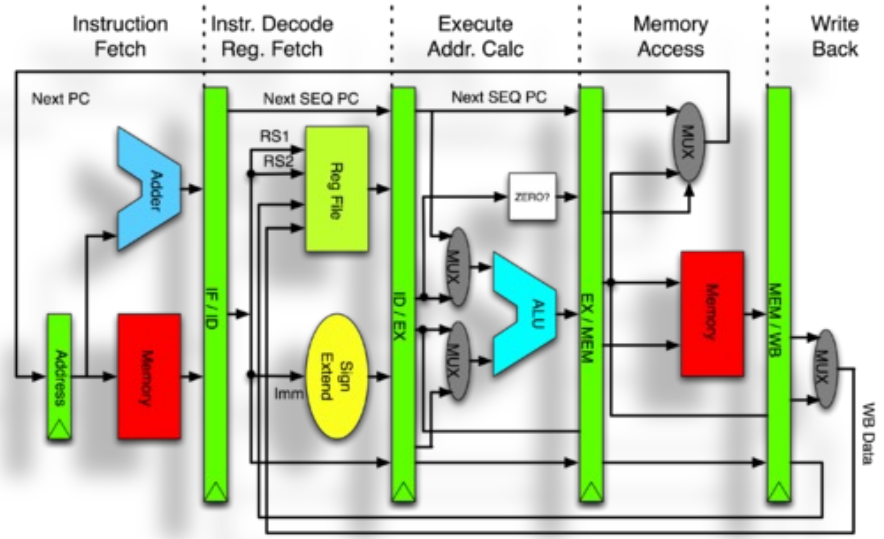
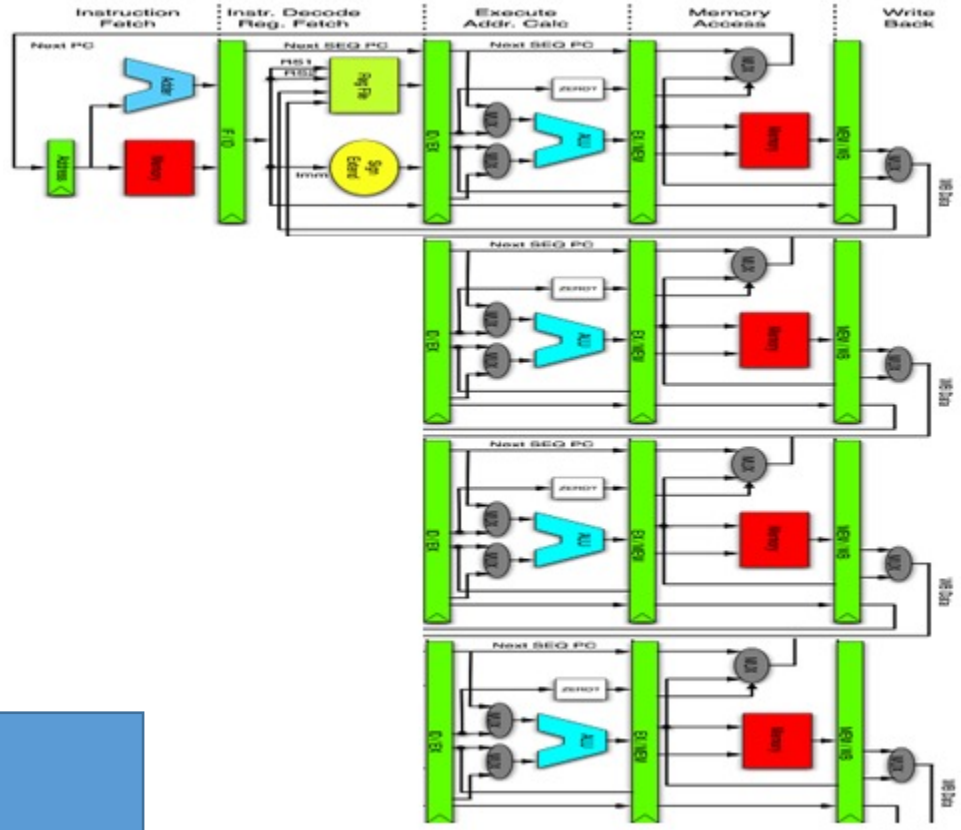




What are the potential bottlenecks here?
When can it improve throughput?

When does vector processing help?





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When can it improve throughput?

Only helps if memory can keep the pipeline busy!

Hardware multi-threading

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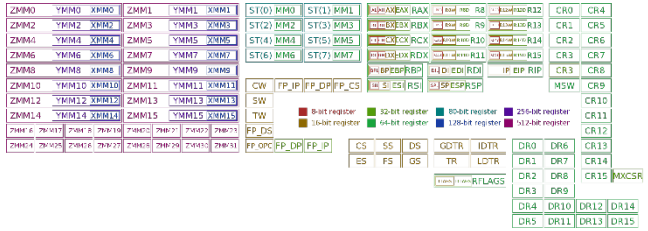

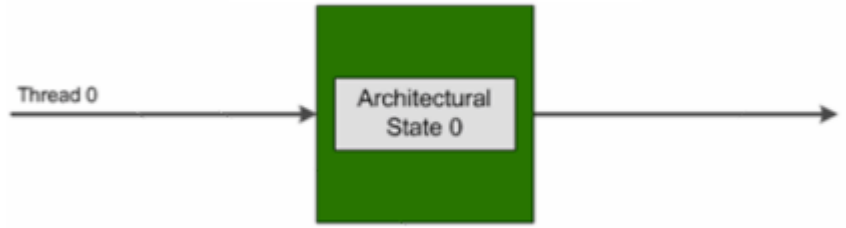

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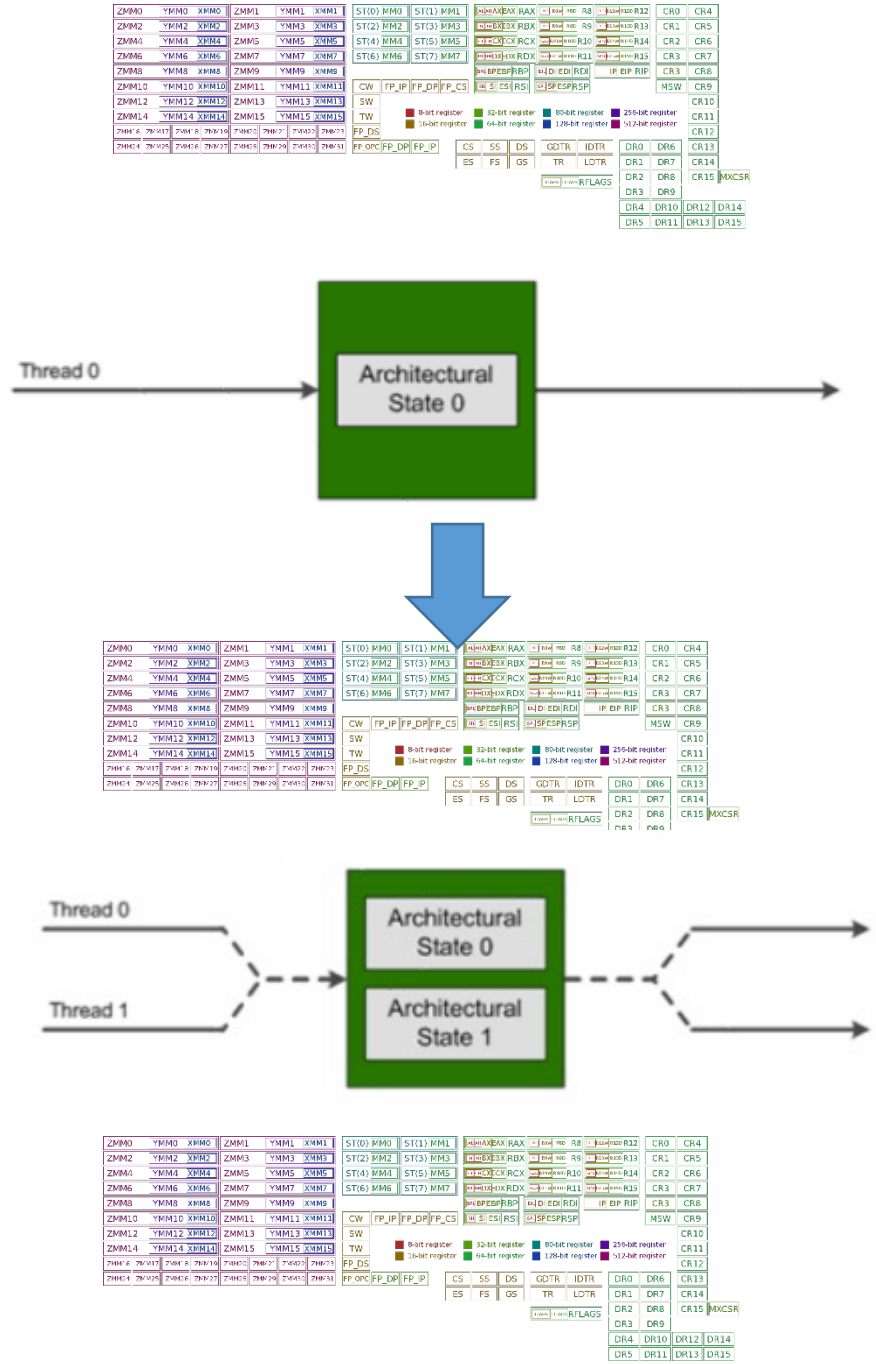

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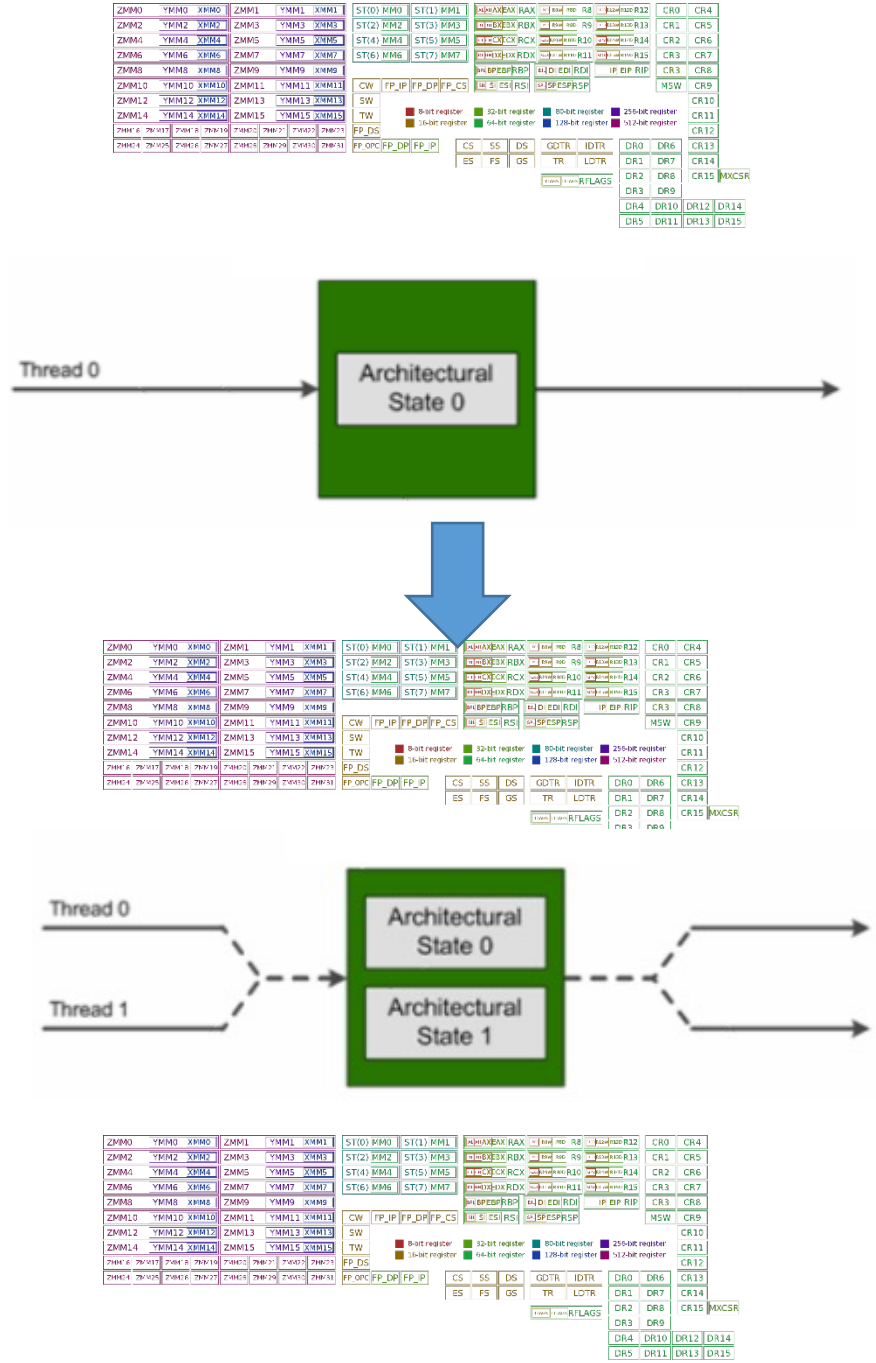
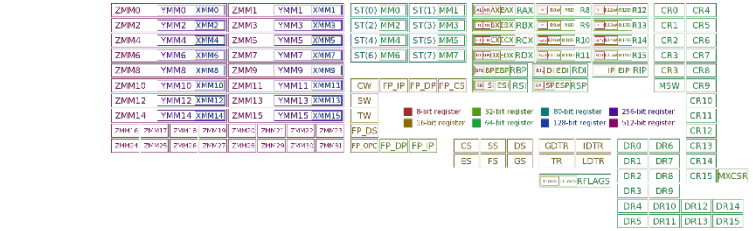
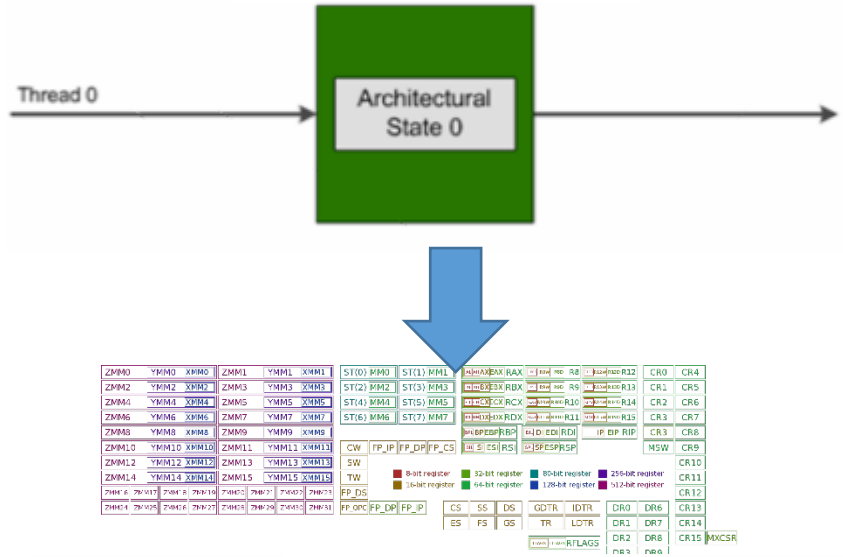
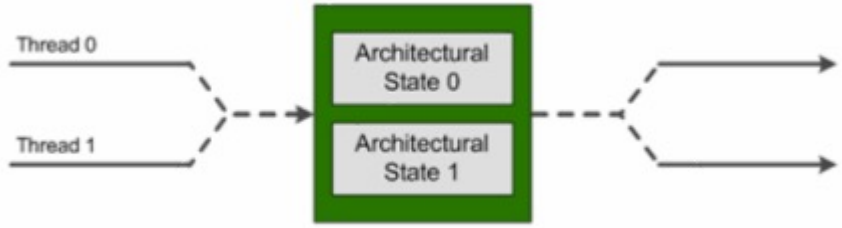


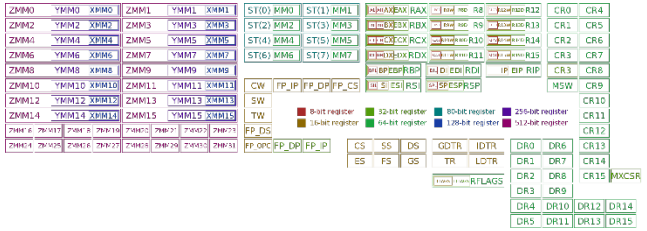
Hardware multi-threading

- Address memory bottleneck
- Share exec unit across
  - Instruction streams
  - Switch on stalls
- Looks like multiple cores to the OS
- Three variants:
  - Coarse
  - Fine-grain
  - Simultaneous



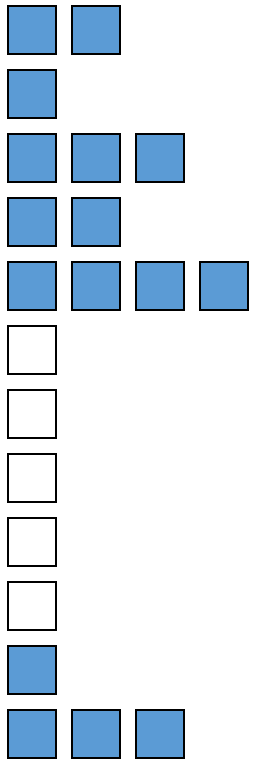




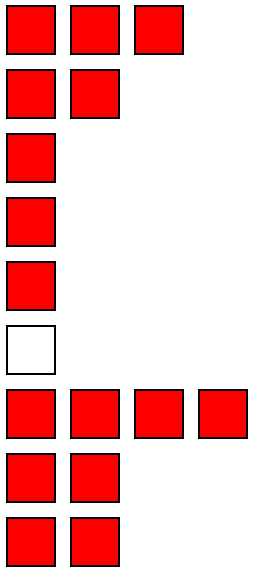


Running example

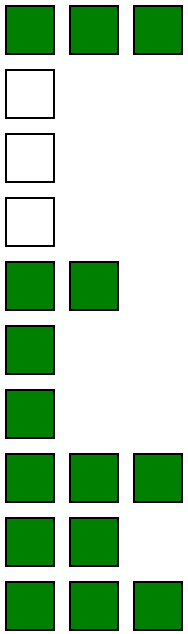
Thread A



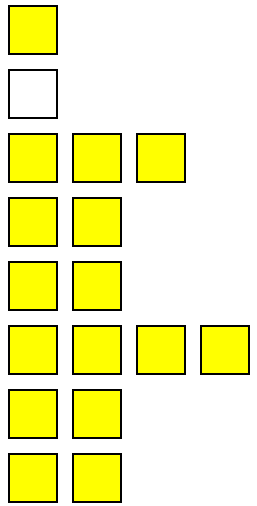
Thread B



Thread C



Thread D



- Colors → pipeline full
- White → stall

Coarse- grained multithreading

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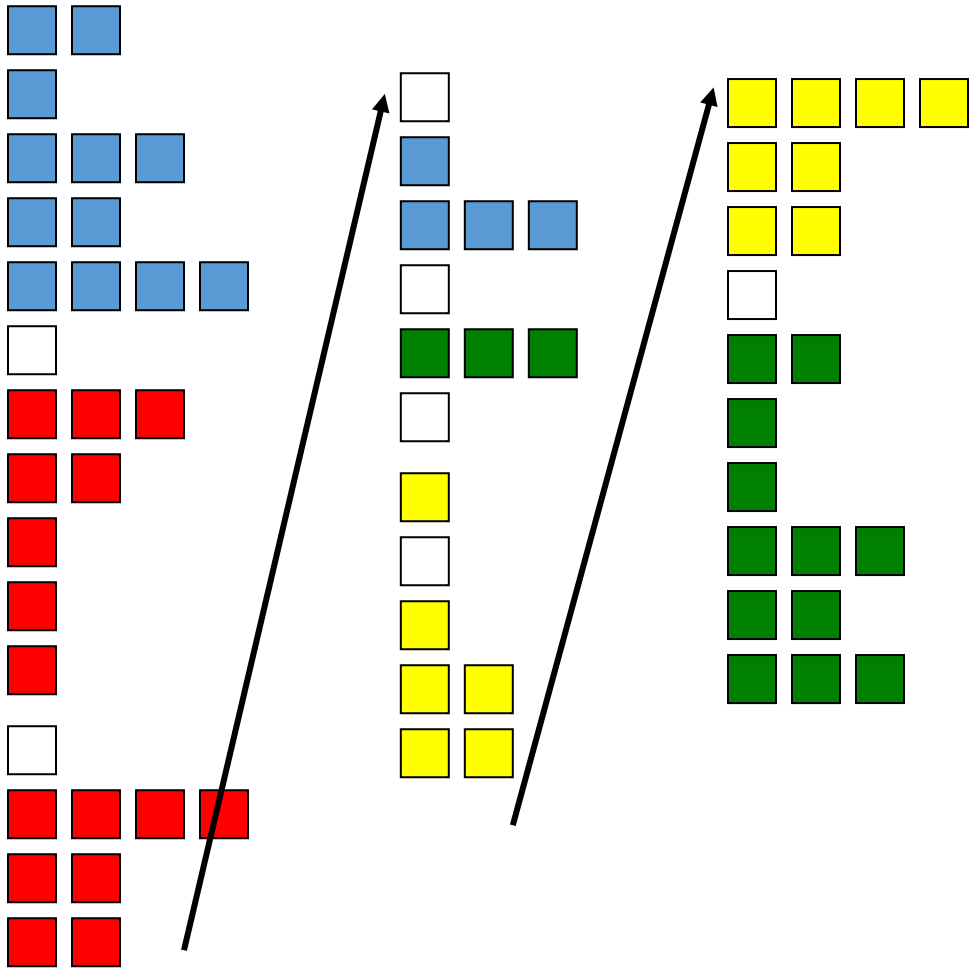

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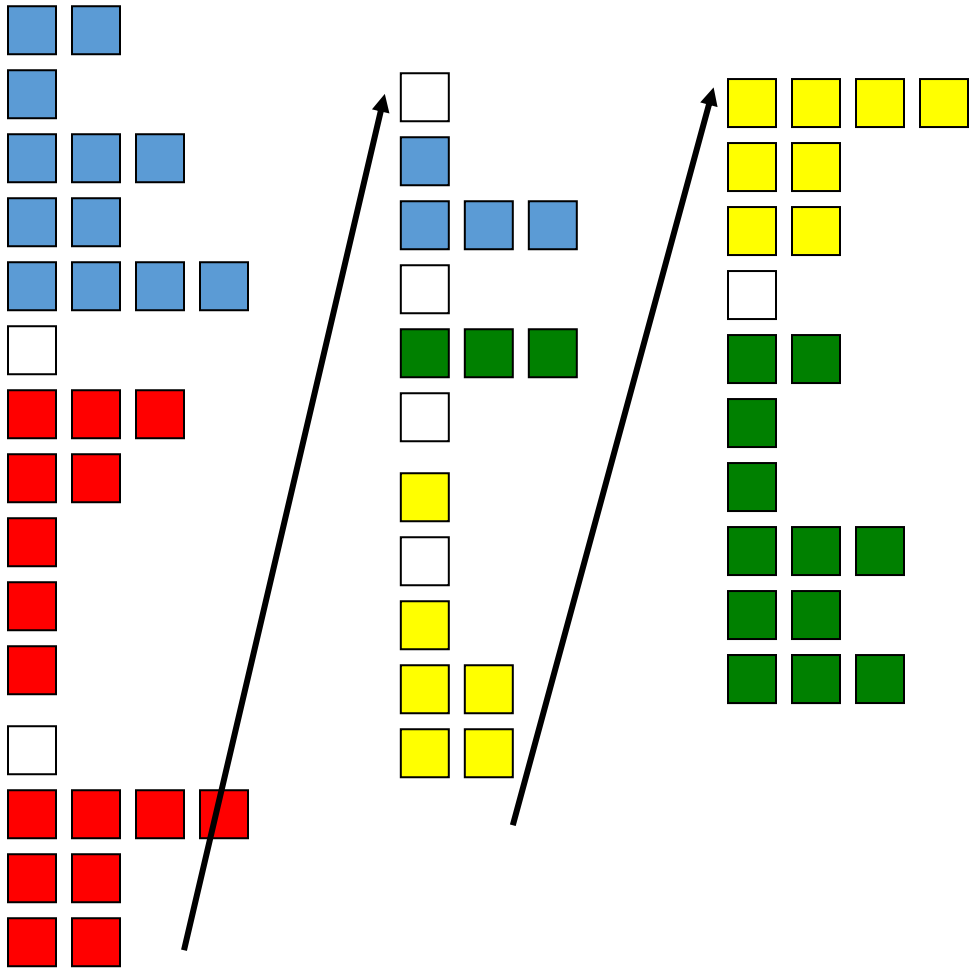

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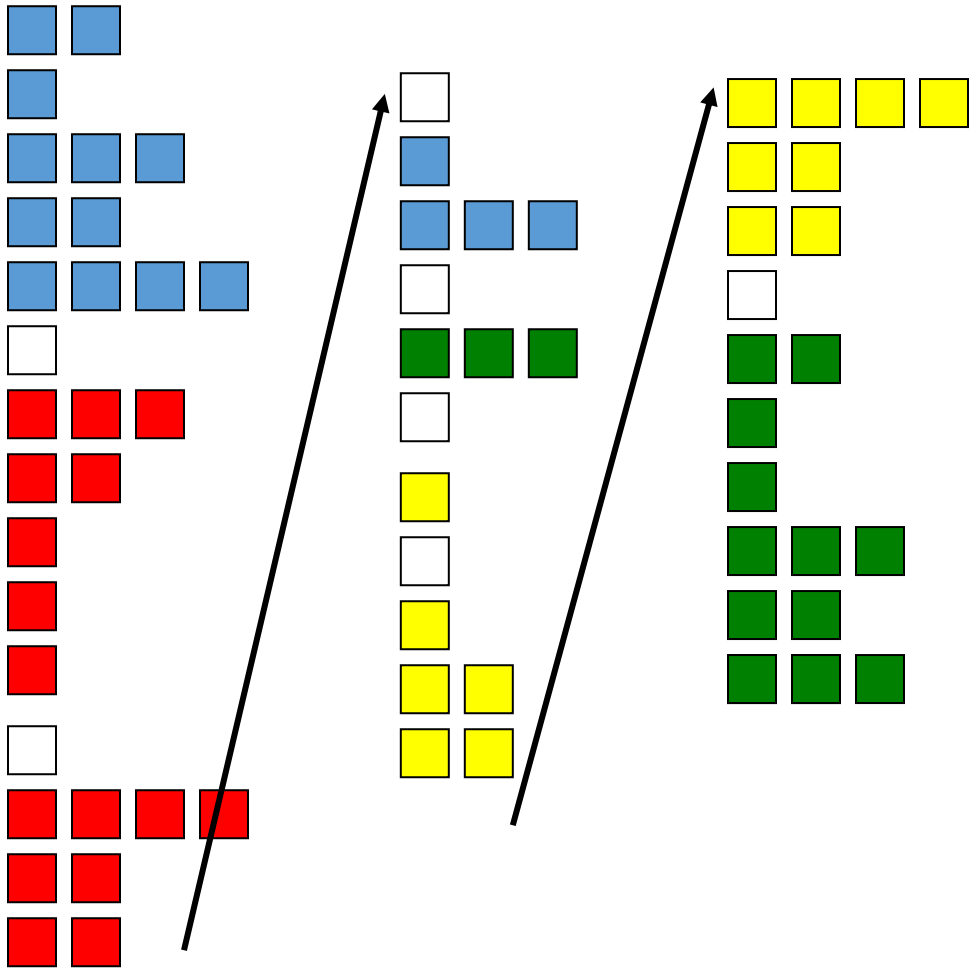

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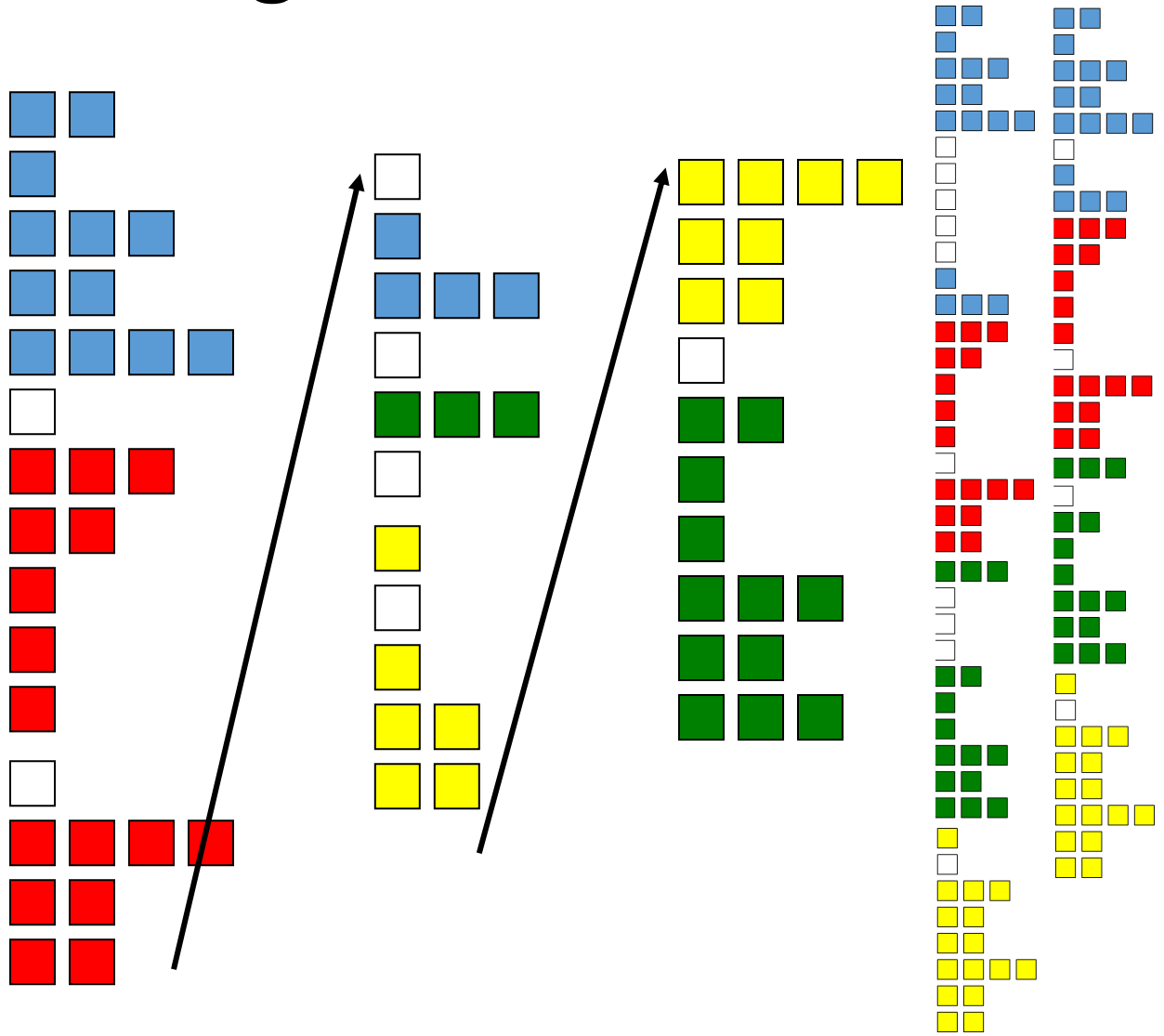

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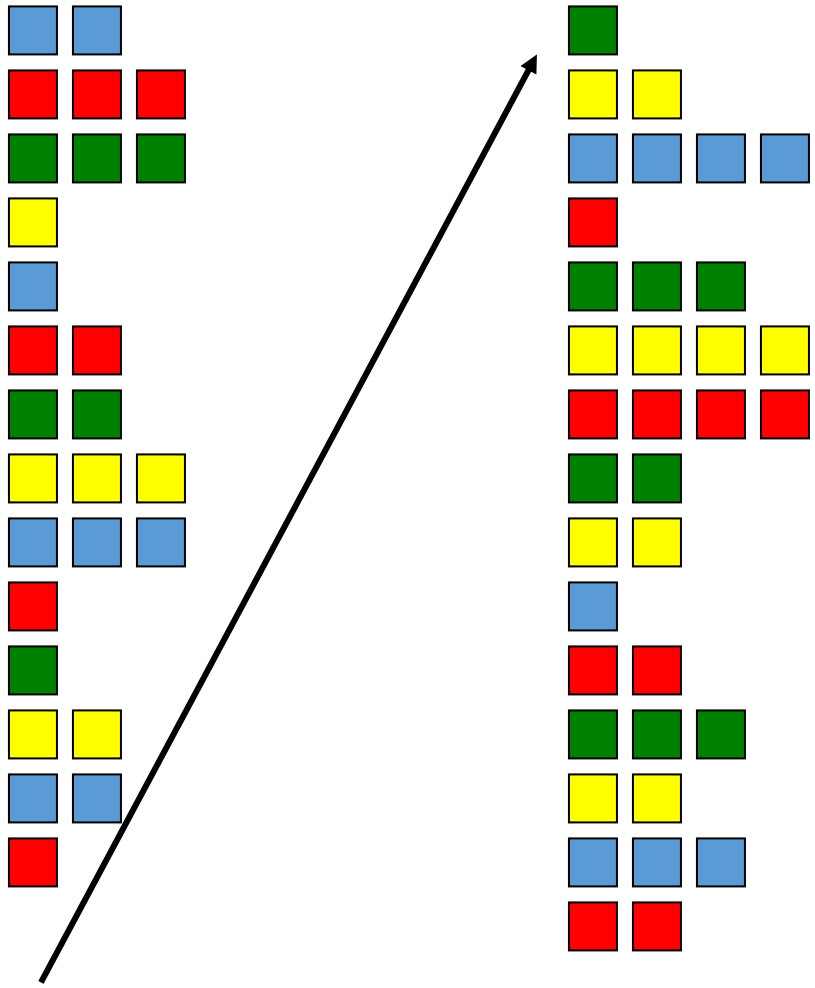

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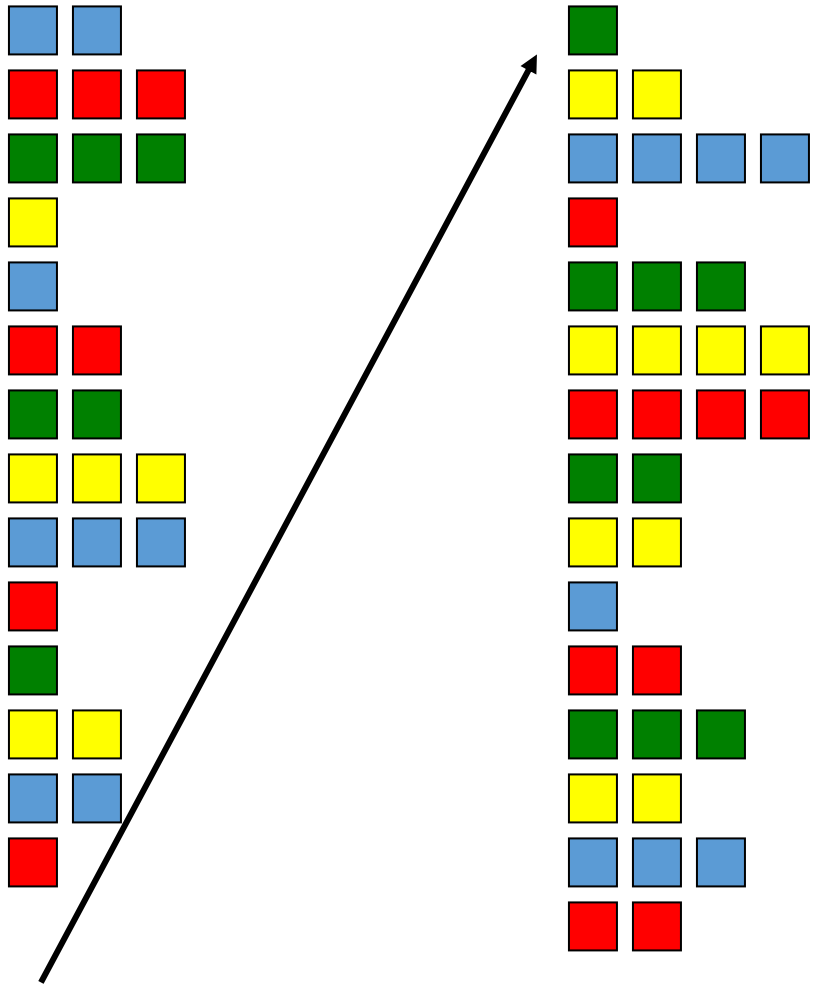

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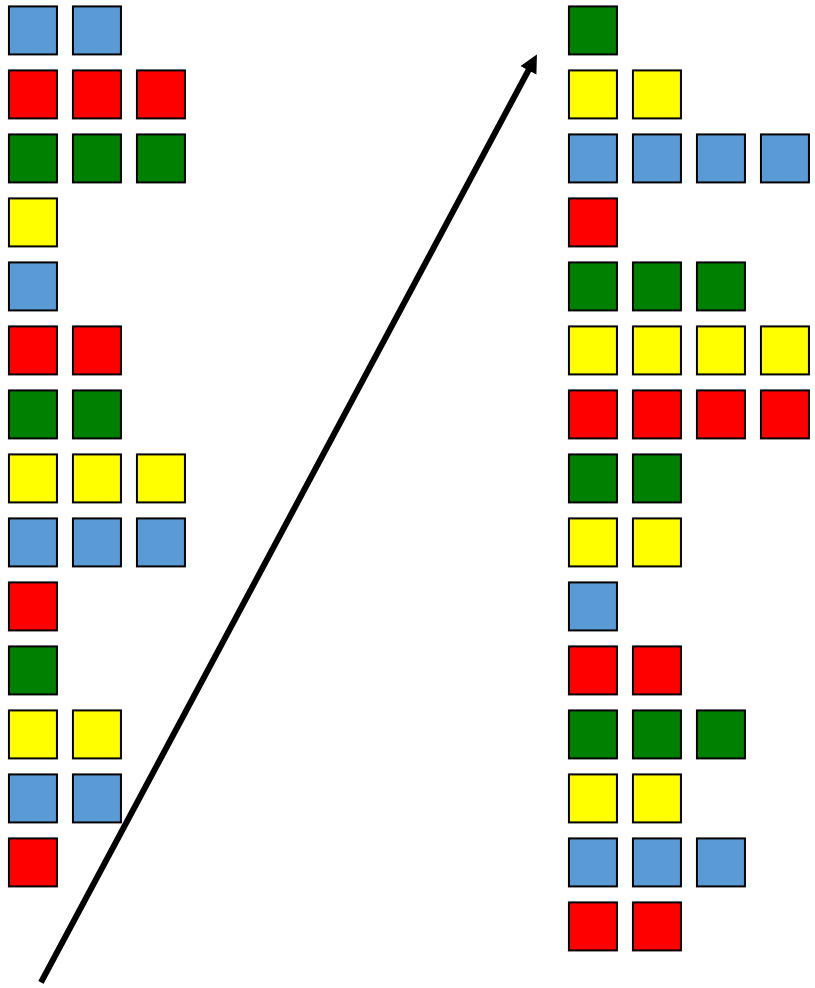

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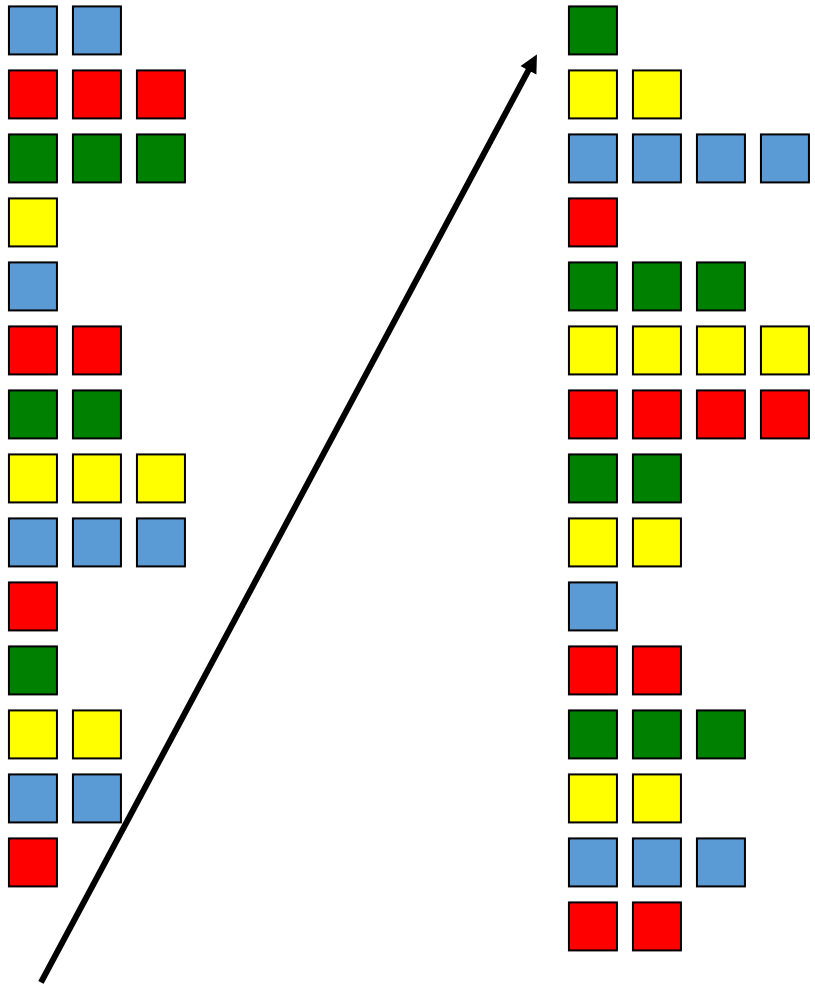

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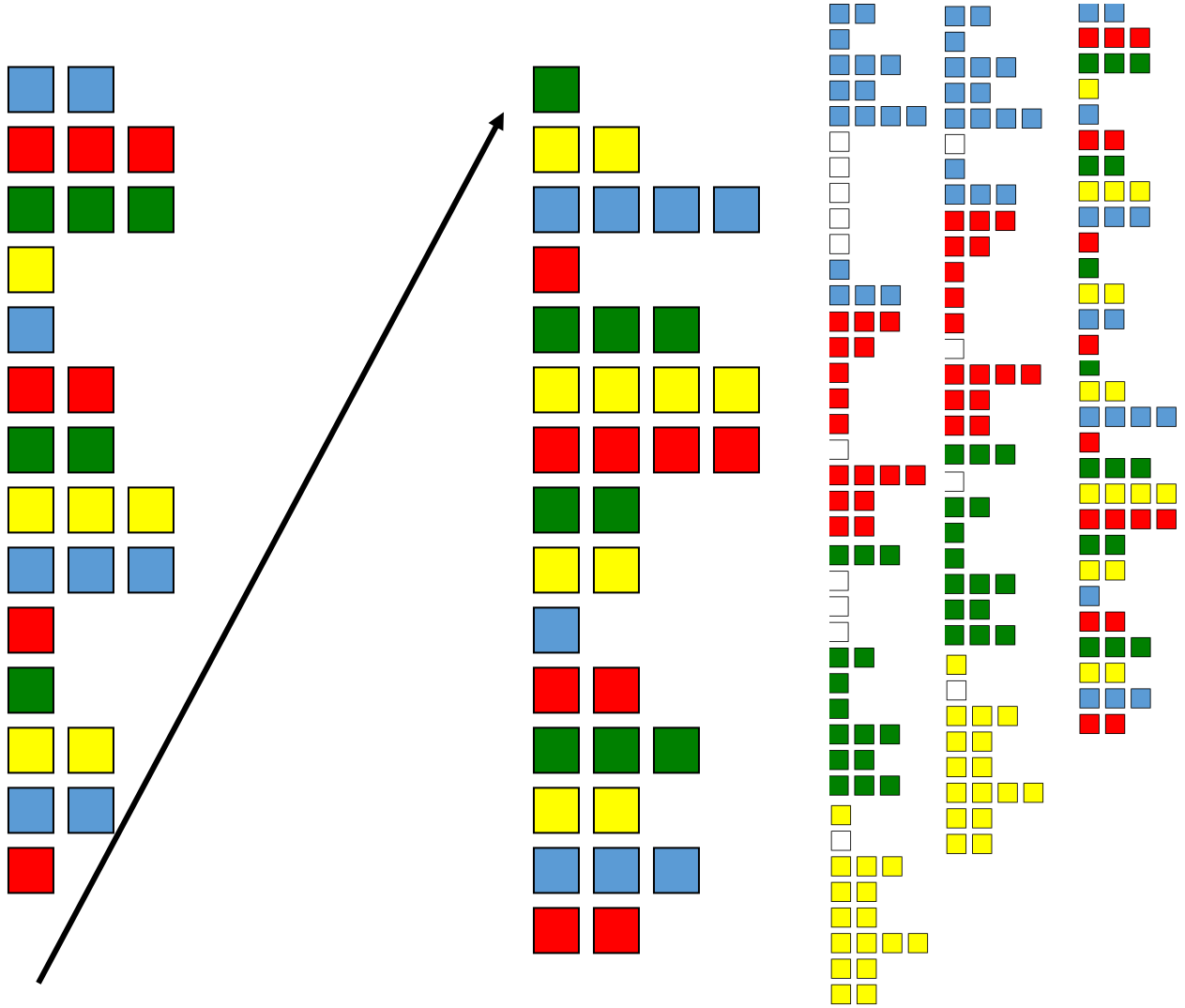

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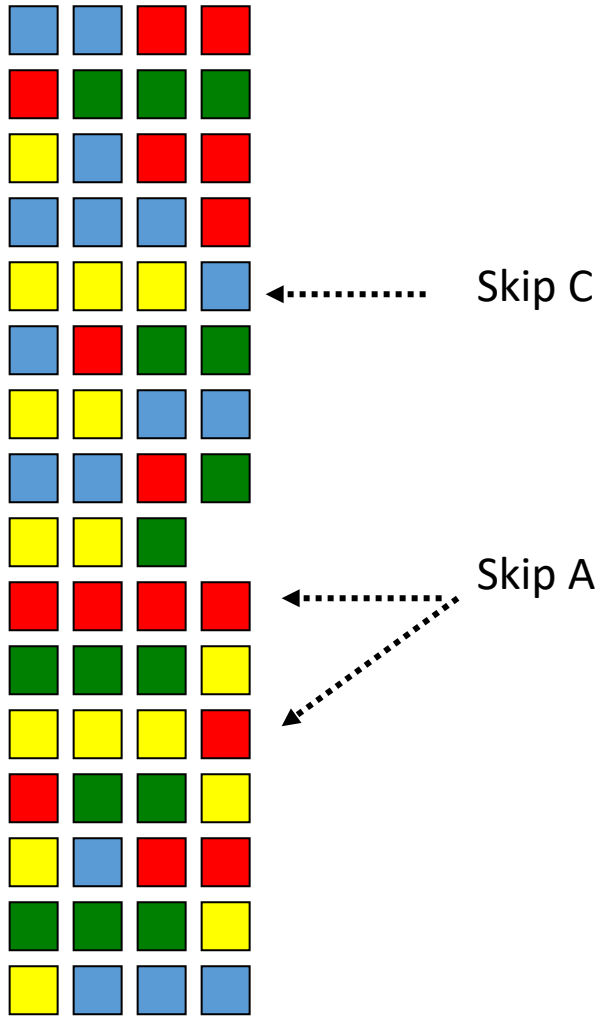

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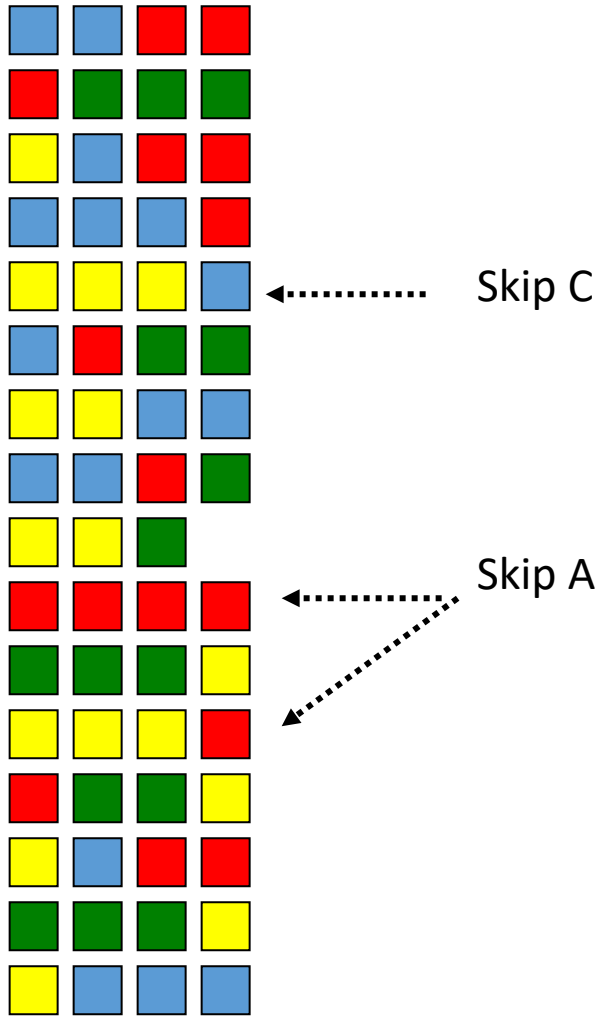

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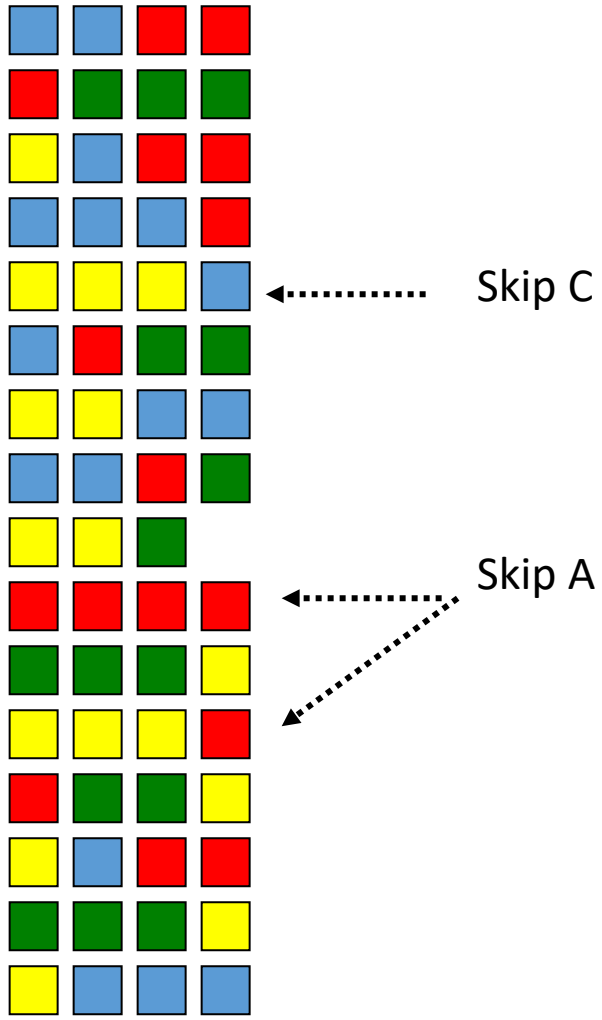

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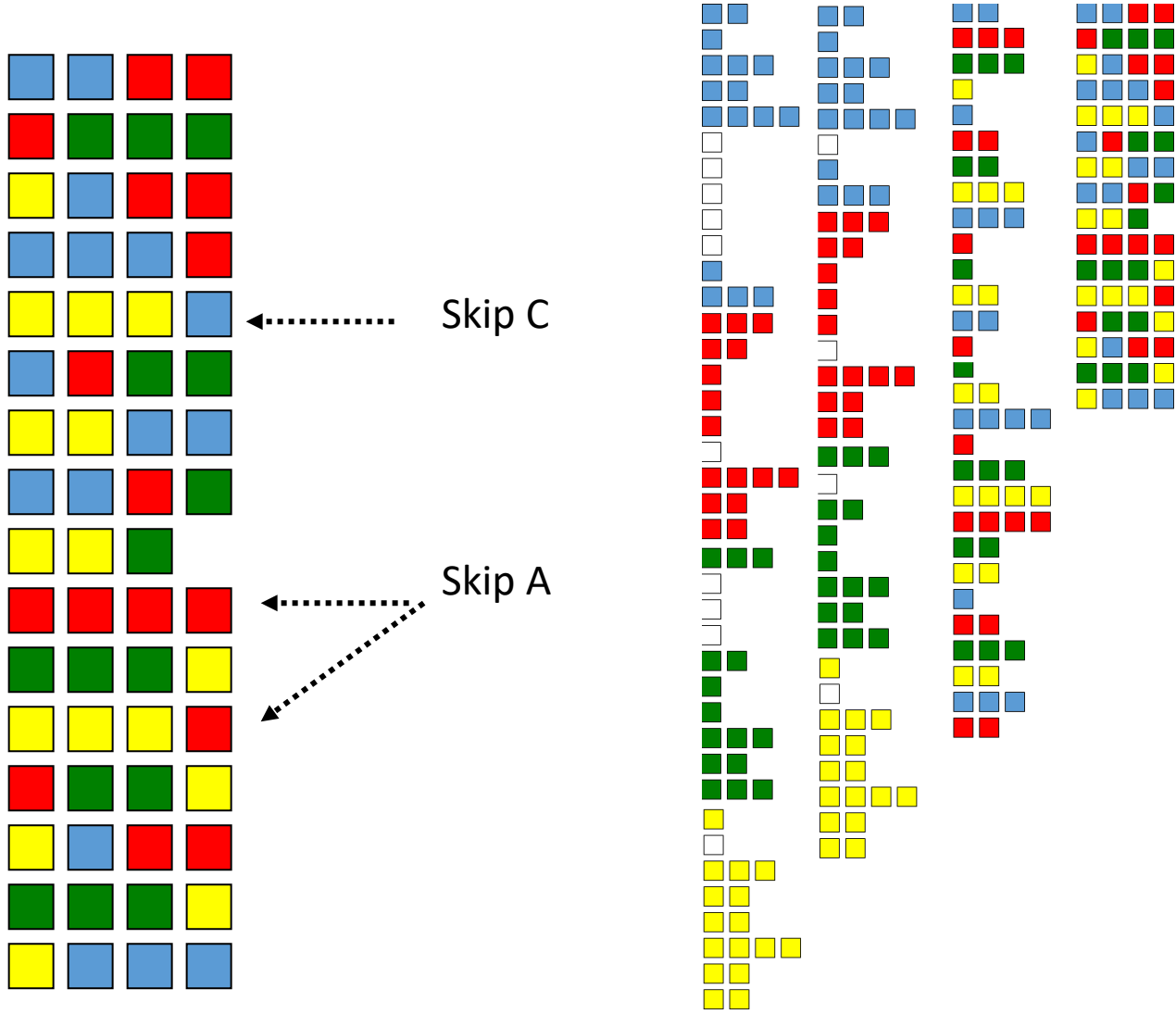

Graphics ~= Rendering

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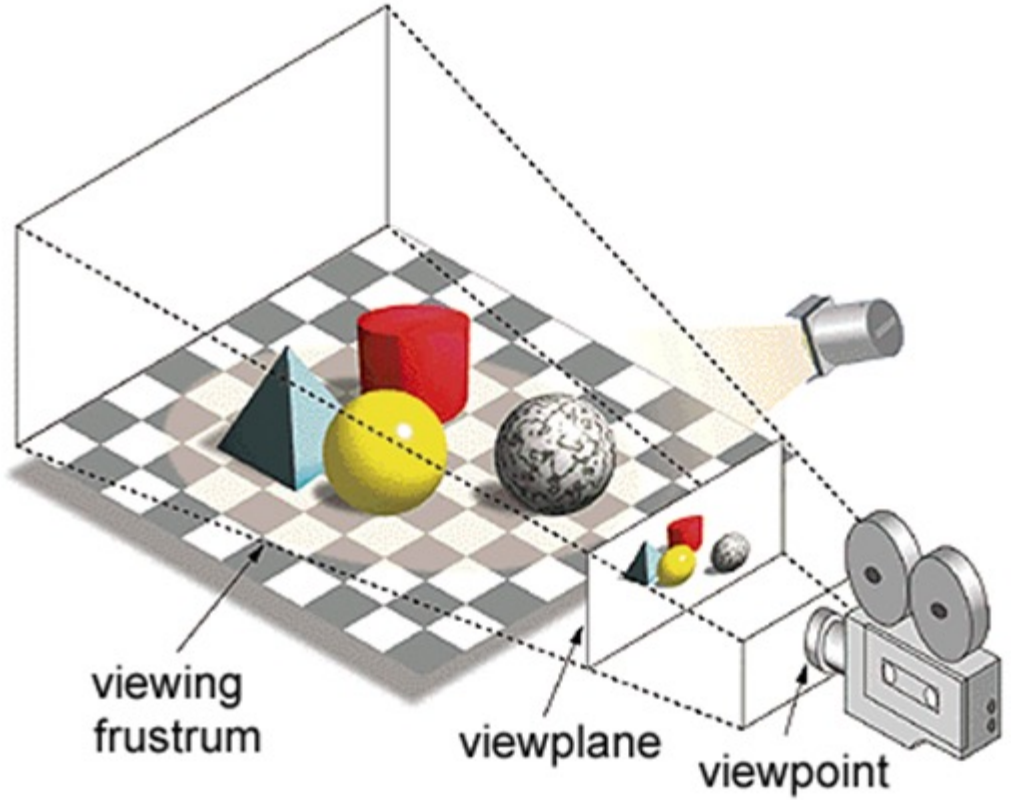

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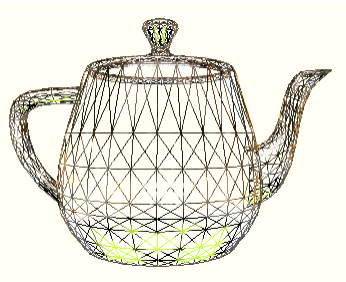

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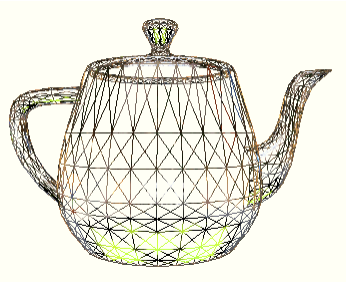

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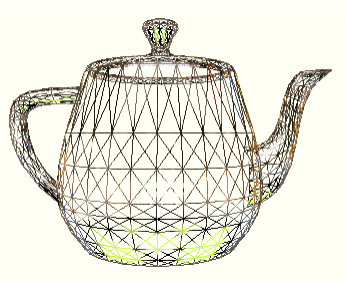

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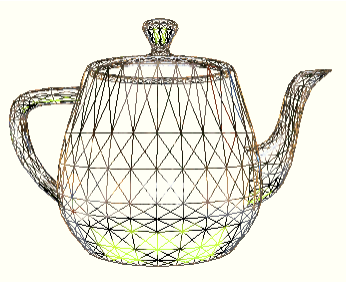

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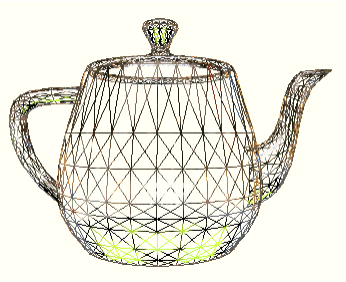

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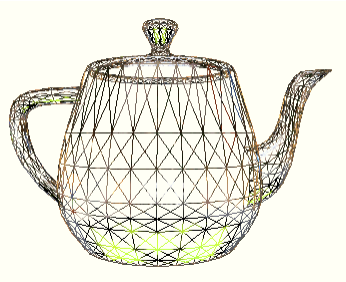

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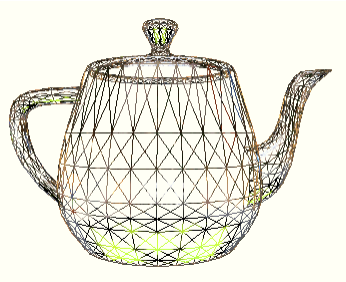

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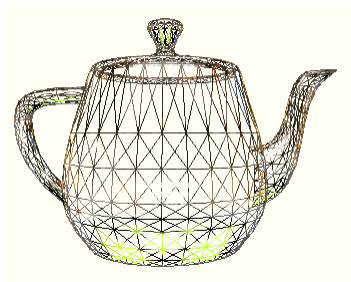

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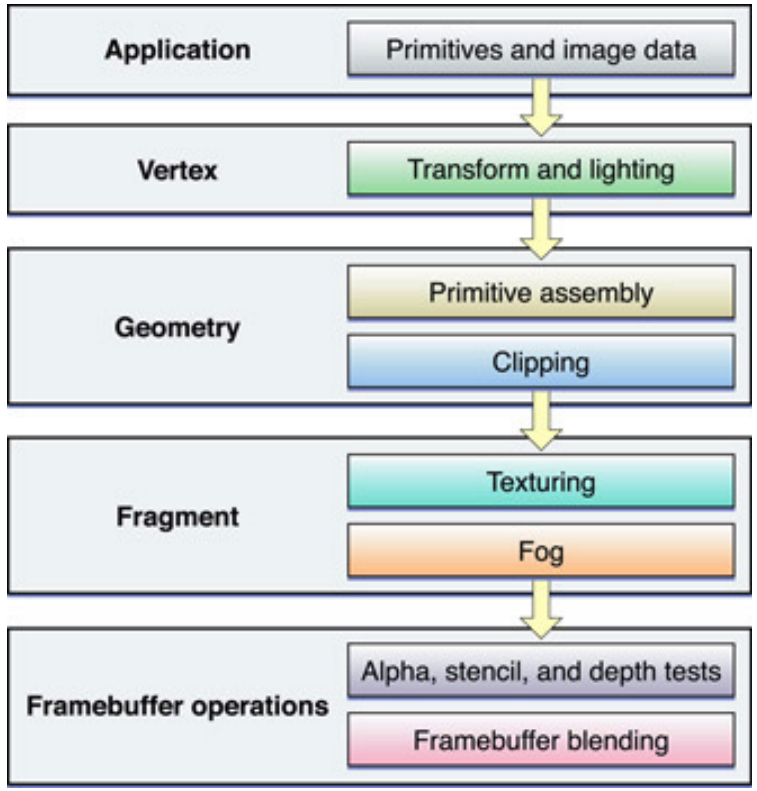

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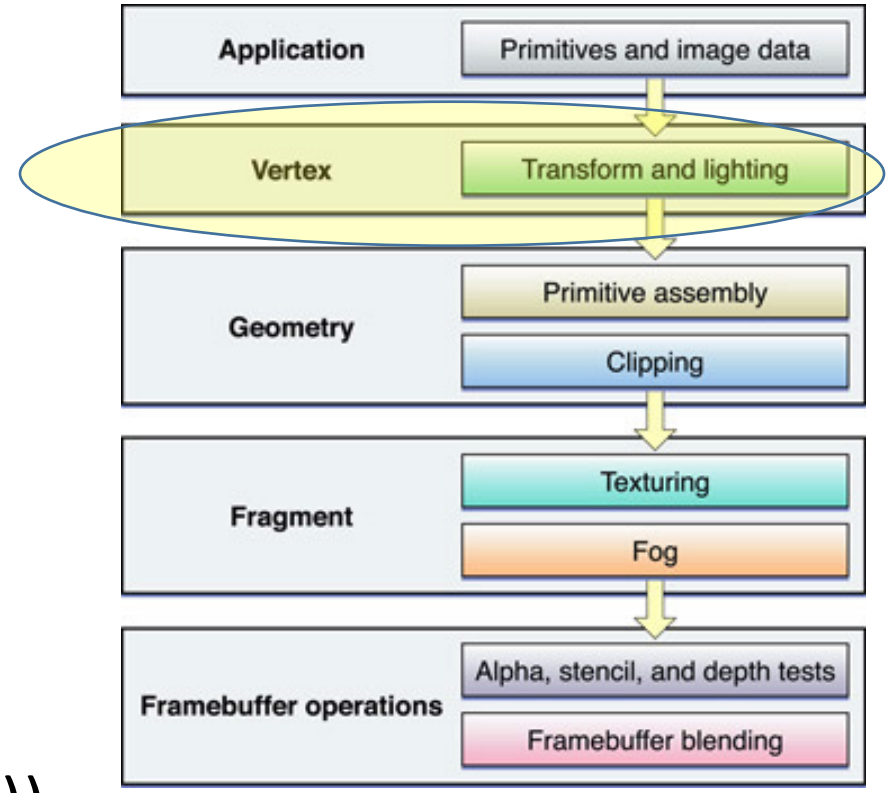

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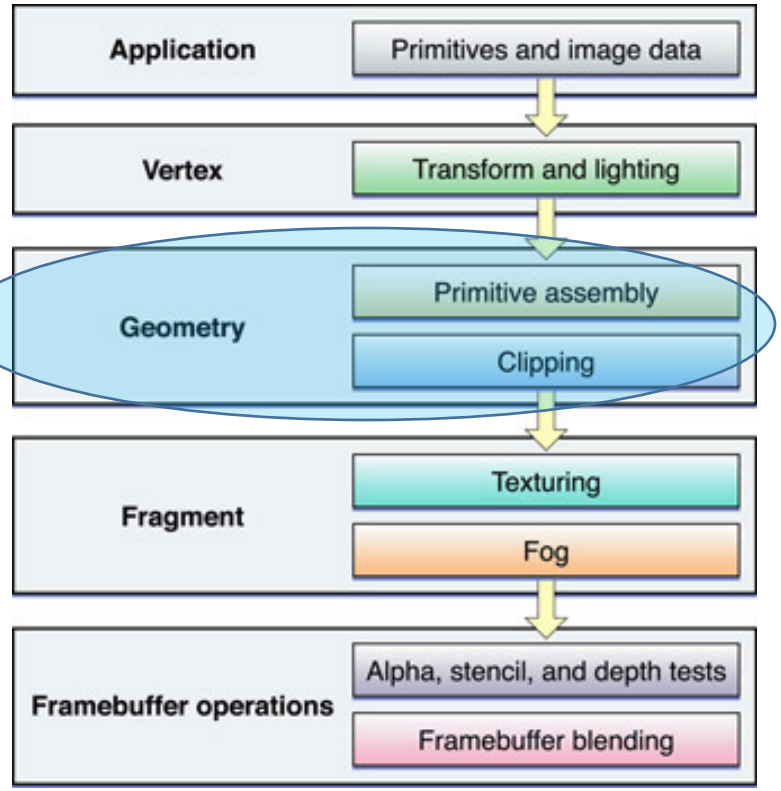

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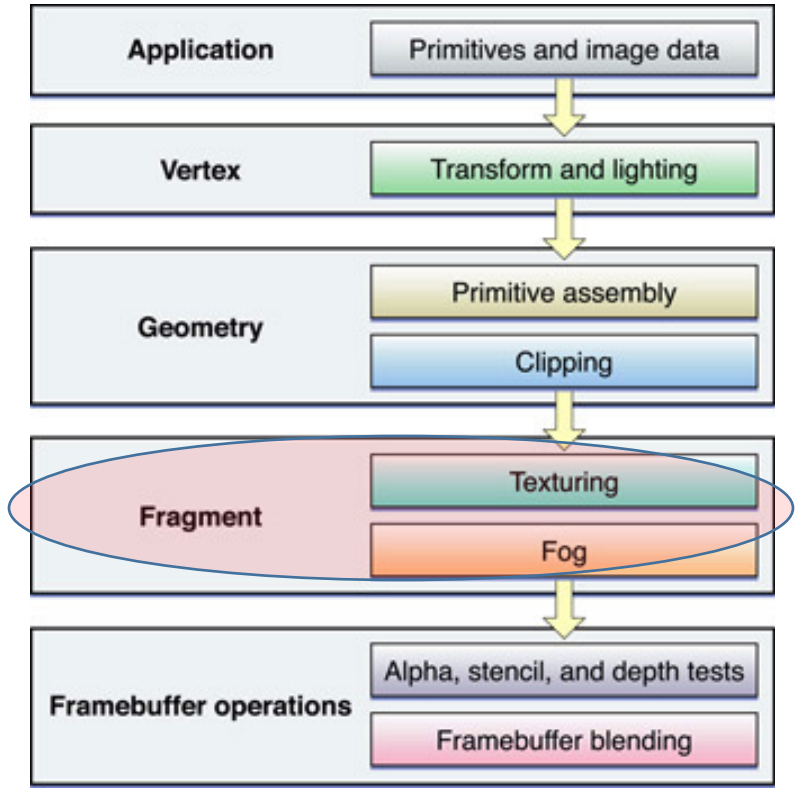

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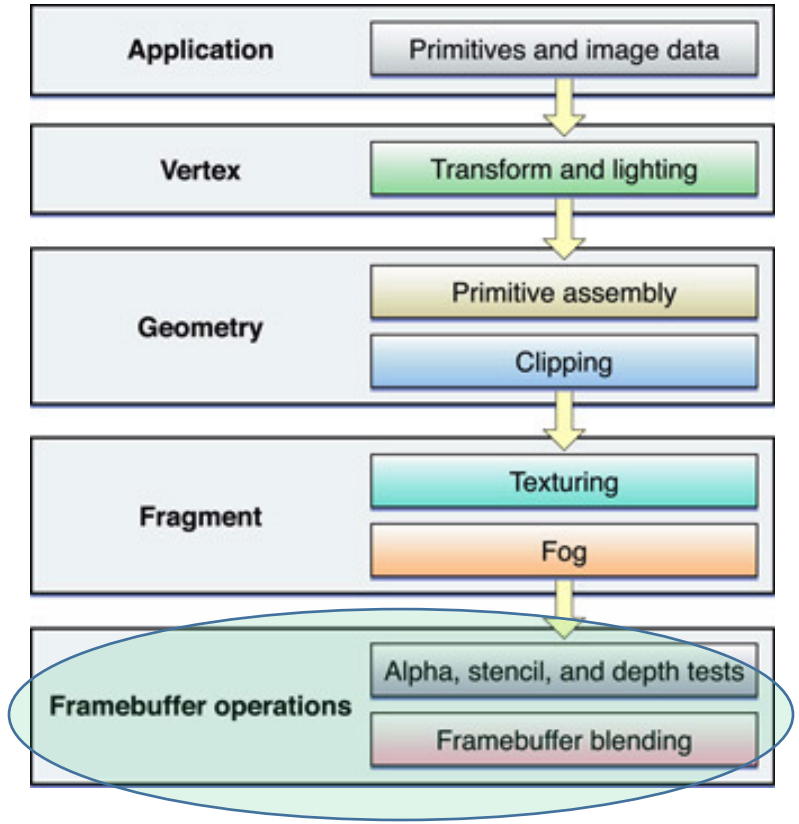

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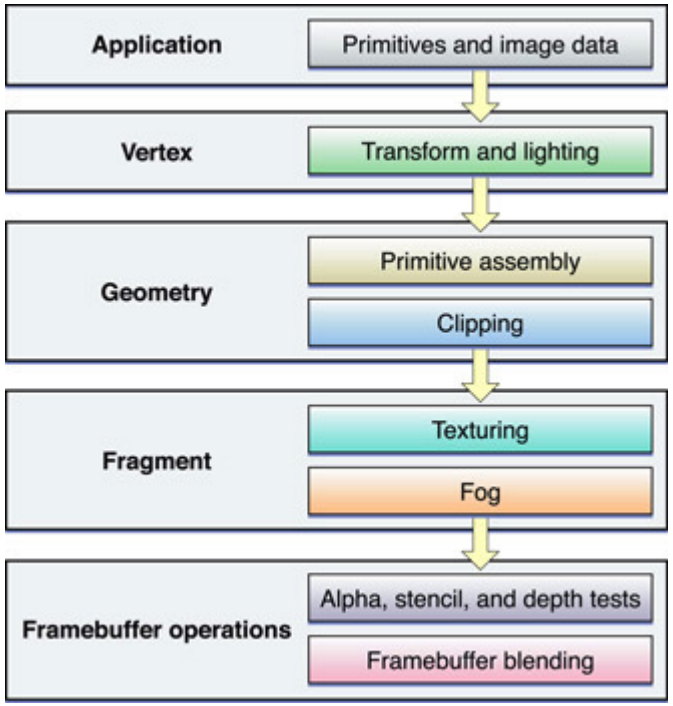
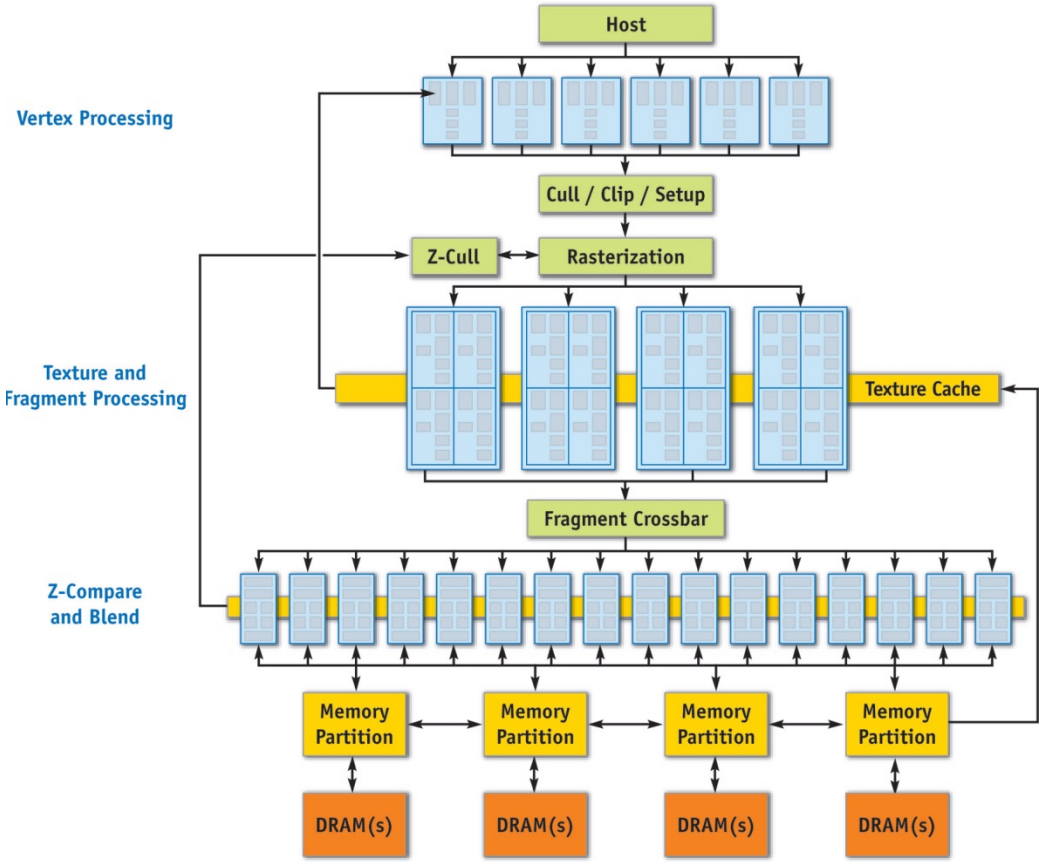
Why Vector and Multithreading Background?

GPU:

- A very wide vector machine
- Massively multi-threaded to hide memory latency
- Originally designed for graphics pipelines…

Graphics pipeline → GPU architecture

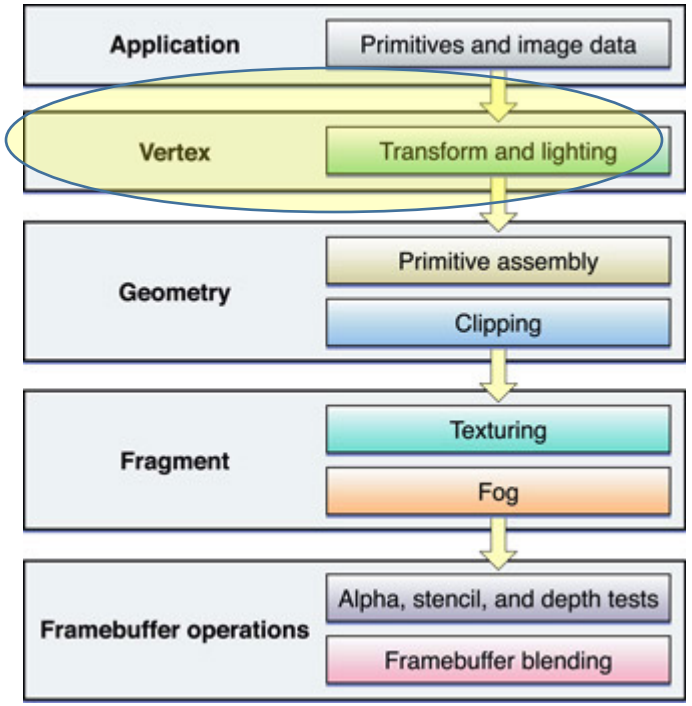


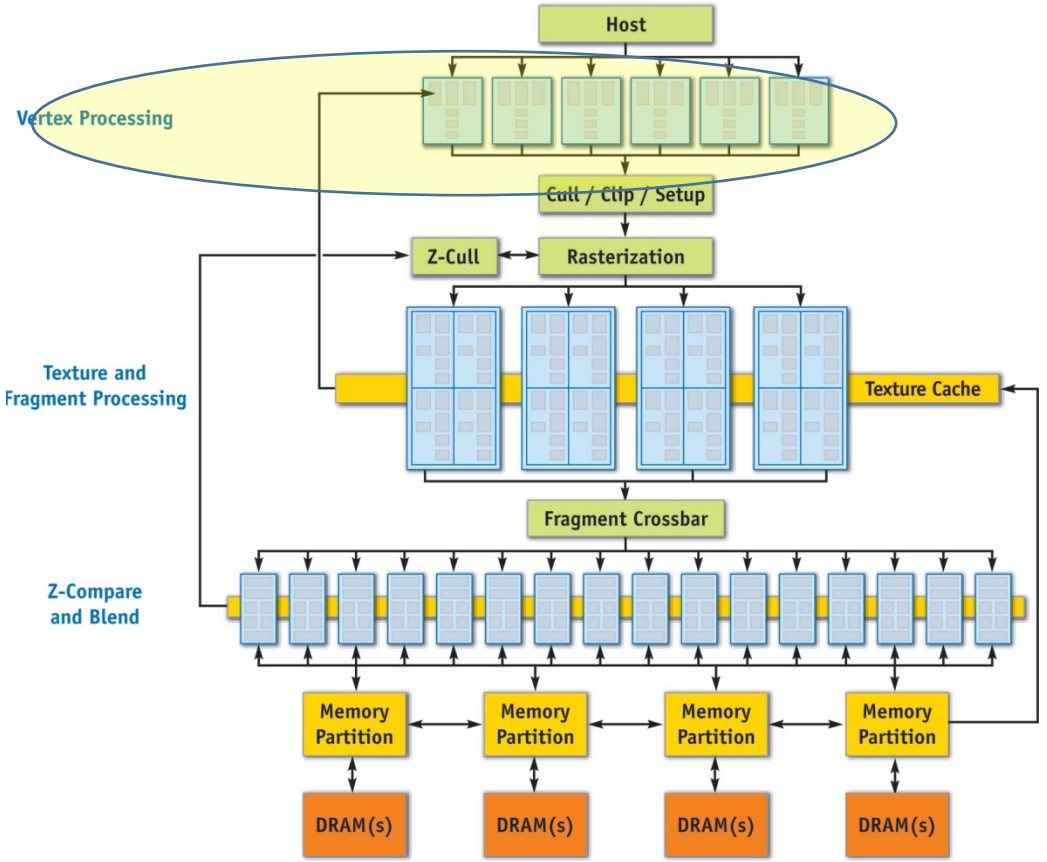


GeForce 6 series

Limited "programmability" of shaders:
Minimal/no control flow
Maximum instruction count

Graphics pipeline → GPU architecture





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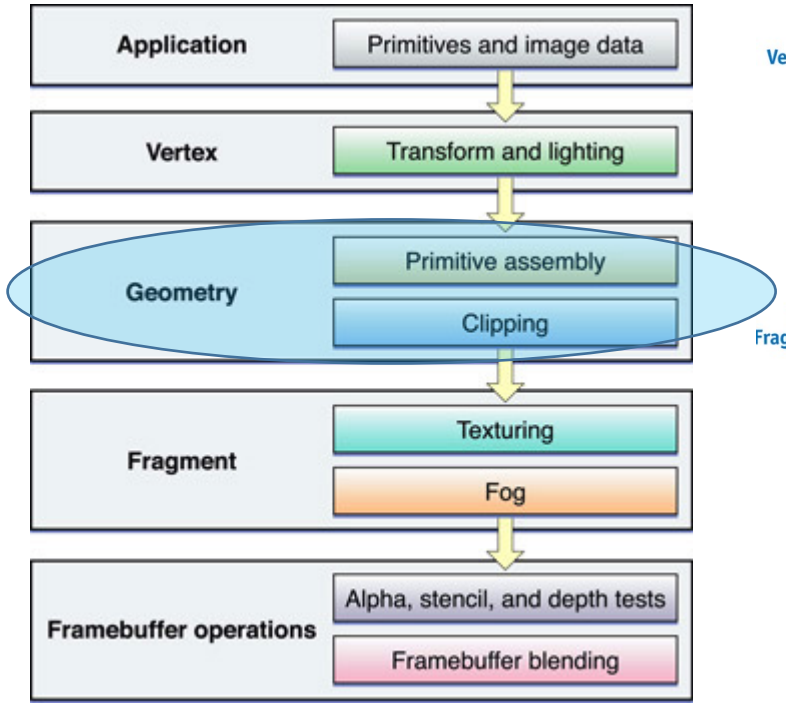

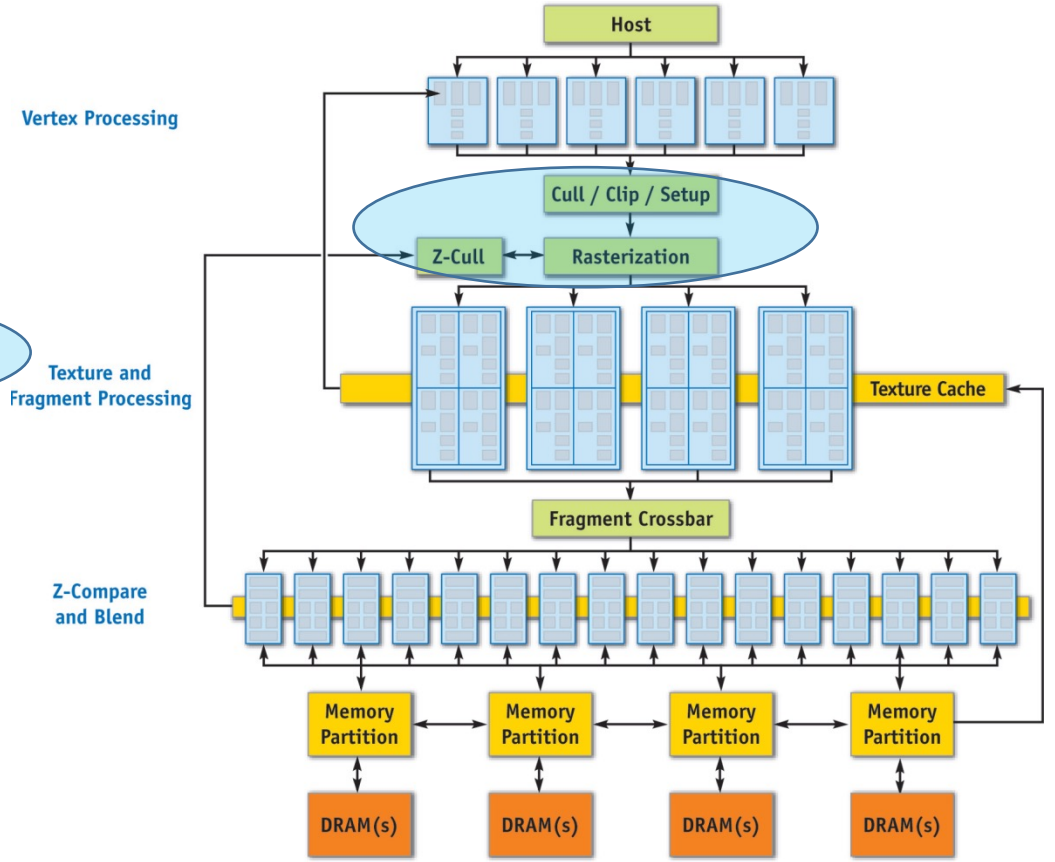

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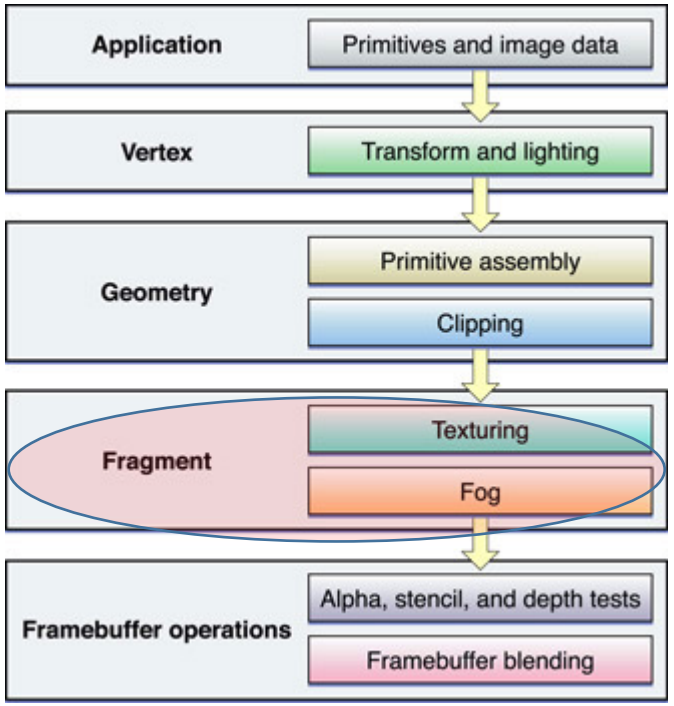

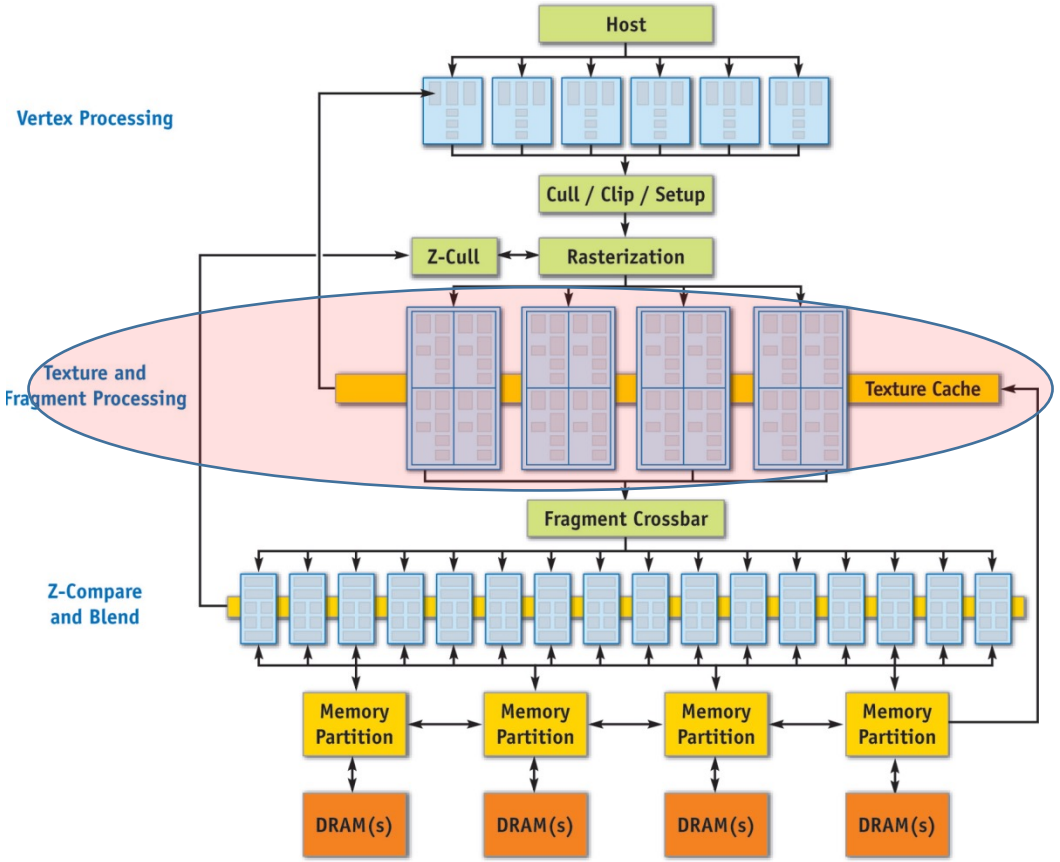

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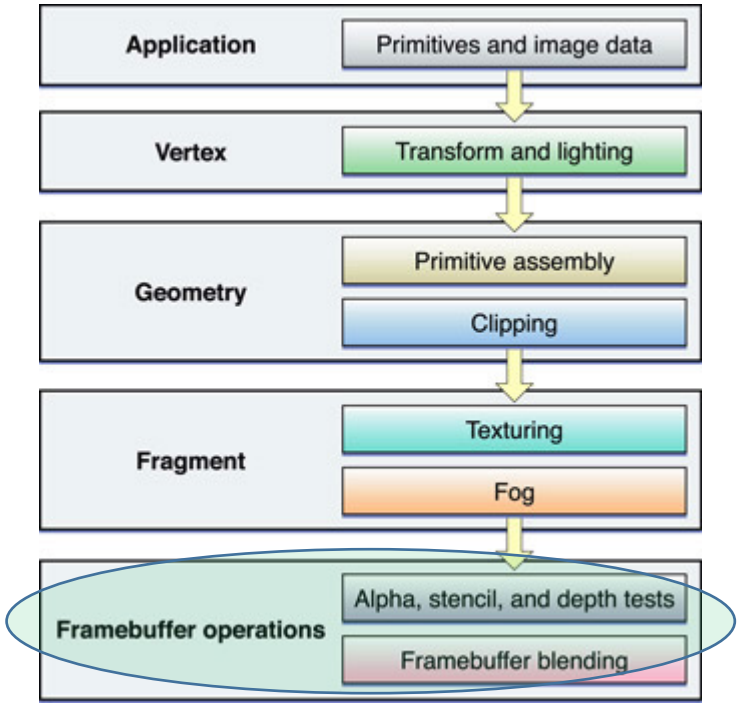

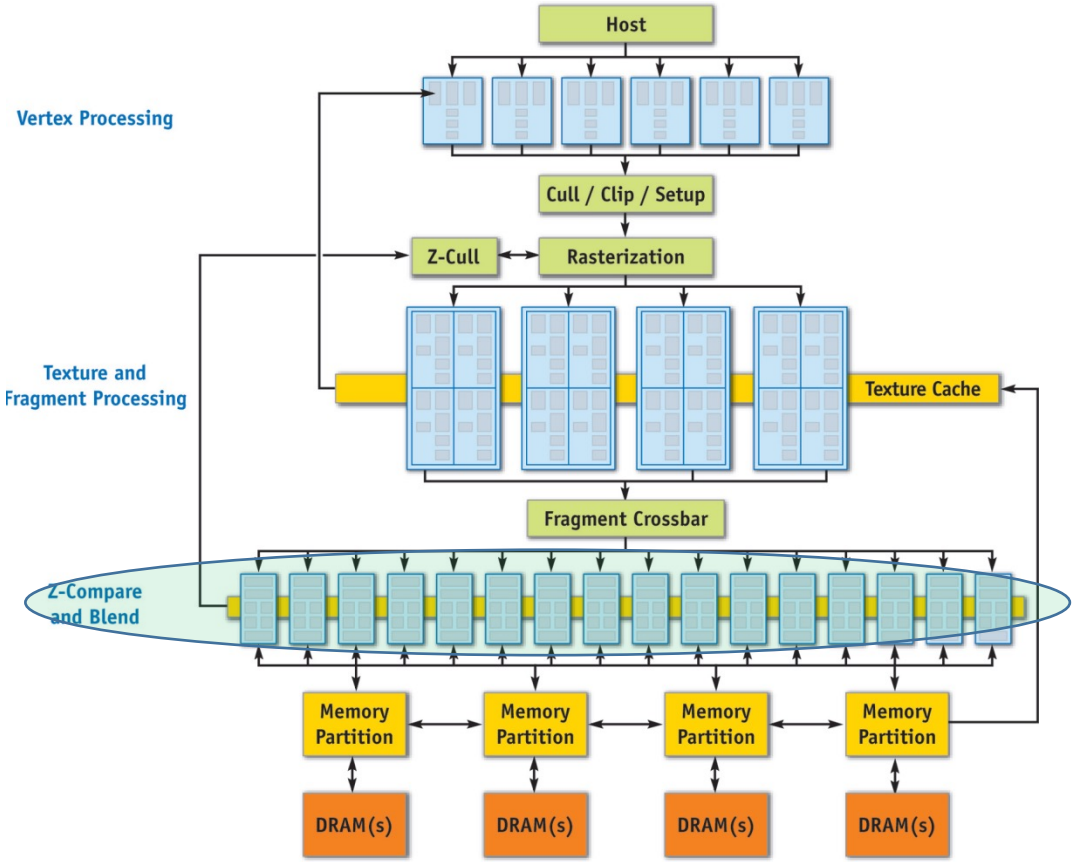

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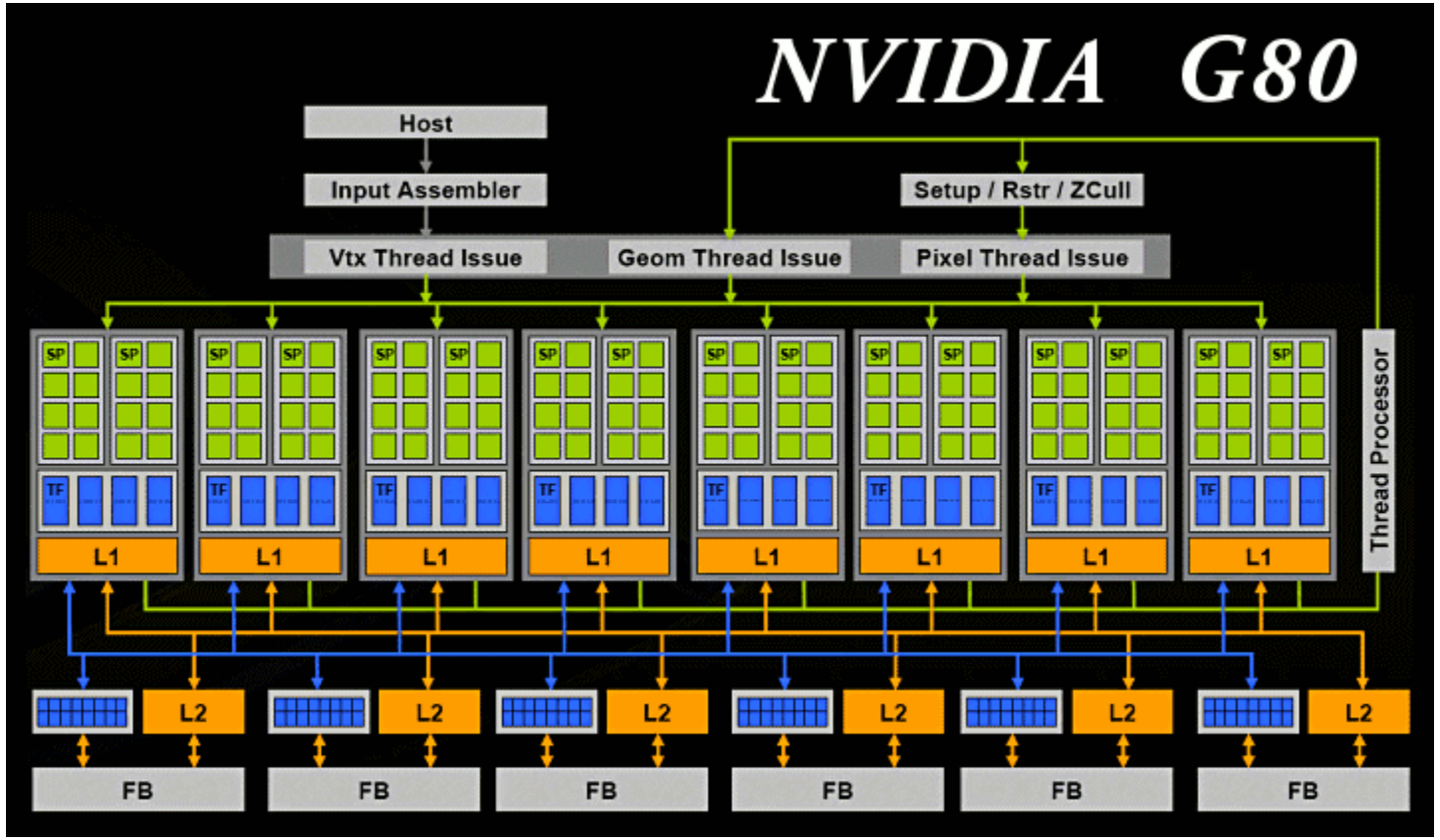
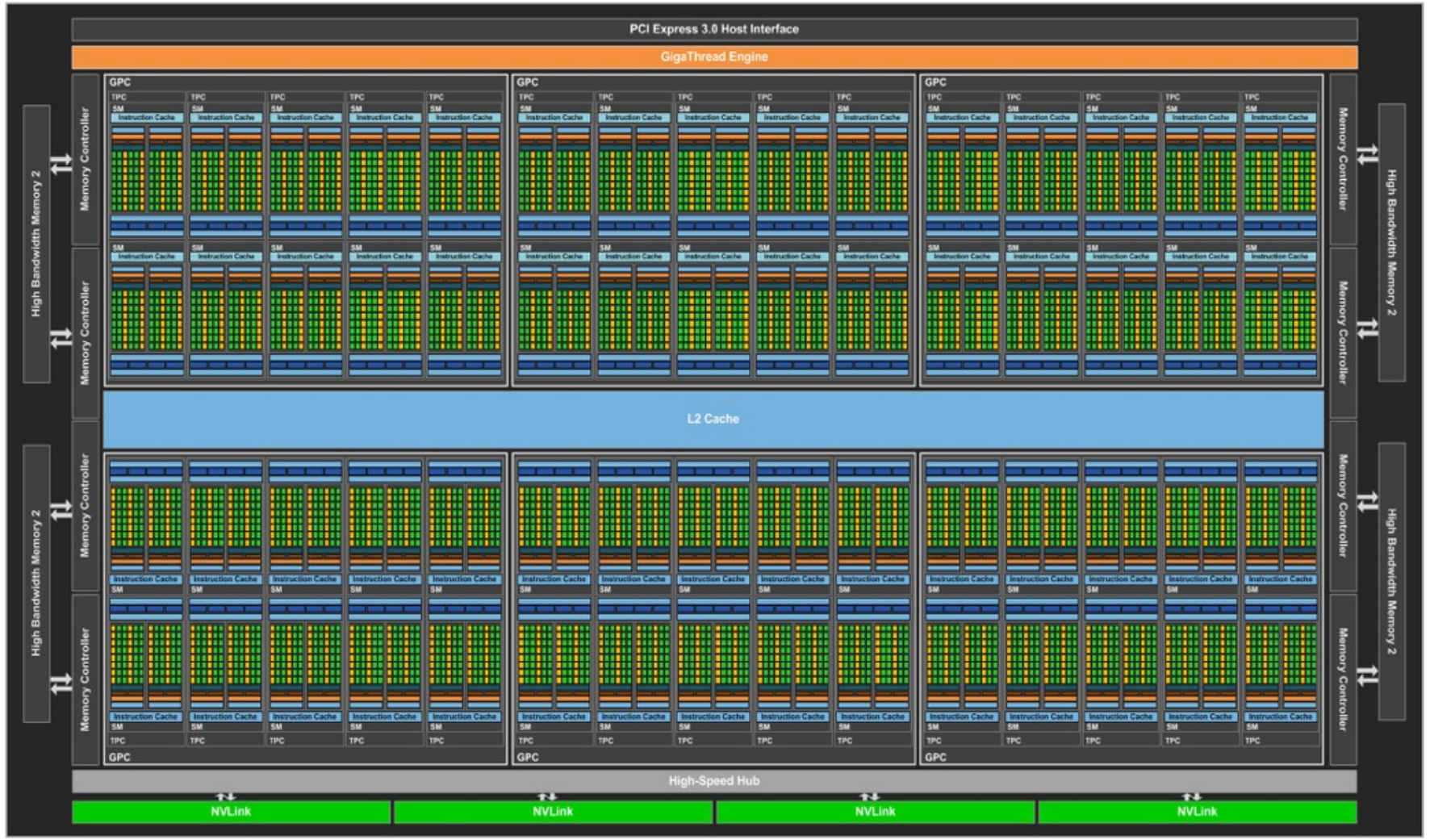
Late Modernity: unified shaders

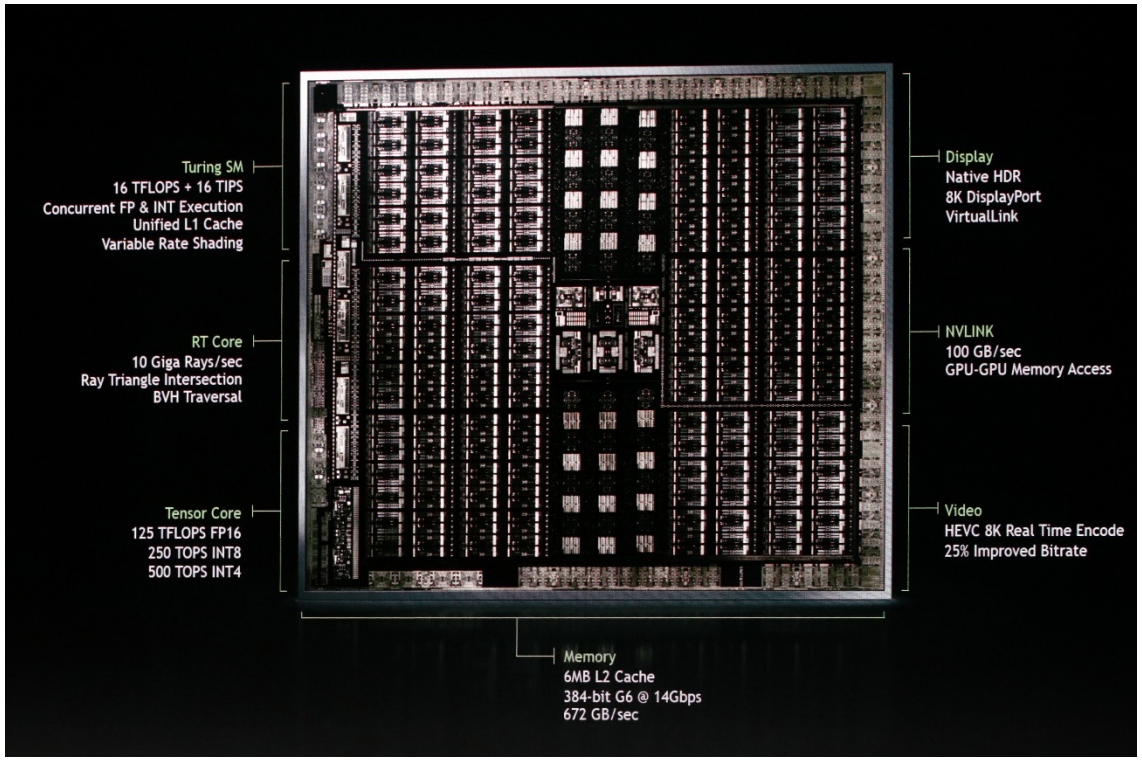


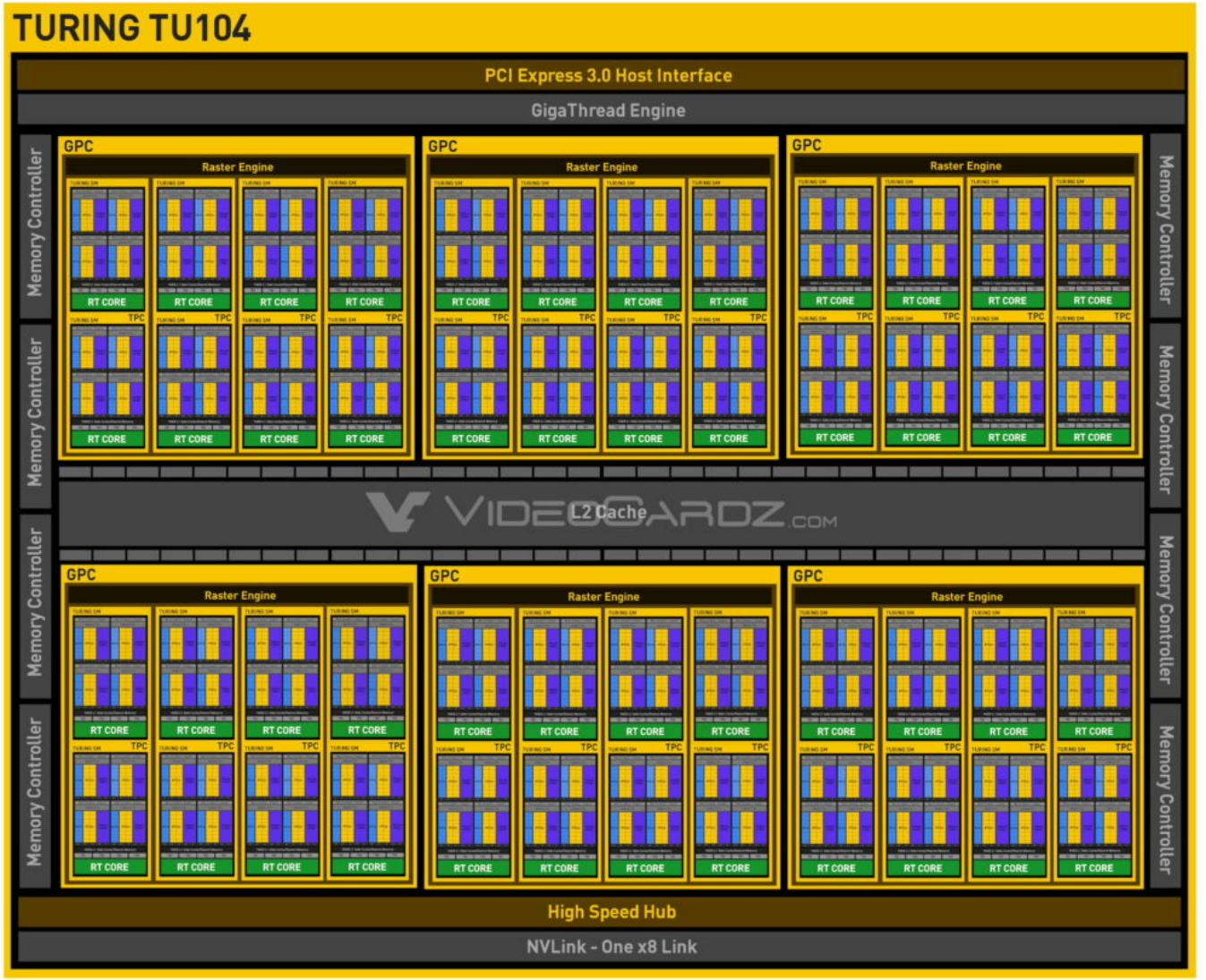
Mapping to Graphics pipeline no longer apparent
Processing elements no longer specialized to a particular role
Model supports *real* control flow, larger instr count

Mostly Modern: Pascal



Definitely Modern: Turing





Modern Enough: Pascal SM

Cross-generational observations

GPUs designed for parallelism in graphics pipeline:

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  - Per-vertex
  - Per-fragment
  - Per-pixel
- Task
  - Vertex processing
  - Fragment processing
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  - Hidden-surface elimination
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But what if my problem isn't painting a box?!!?!

The big ideas still present in GPUs

- Simple cores
- Single instruction stream
  - Vector instructions (SIMD) OR
  - Implicit HW-managed sharing (SIMT)
- Hide memory latency with HW multi-threading

Programming Model

- ***GPUs are I/O devices, managed by user-code***
- “kernels” == “shader programs”
- 1000s of HW-scheduled threads per kernel
- Threads grouped into independent blocks.
  - Threads in a block can synchronize (barrier)
  - This is the *only* synchronization
- “Grid” == “launch” == “invocation” of a kernel
  - a group of blocks (or warps)

Parallel Algorithms

- Sequential algorithms often do not permit easy parallelization
  - Does not mean there work has no parallelism
  - A different approach can yield parallelism
  - but often changes the algorithm
  - Parallelizing != just adding locks to a sequential algorithm
- Parallel Patterns
  - Map
  - Scatter, Gather
  - Reduction
  - Scan
  - Search, Sort

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  - Reduction
  - Scan
  - Search, Sort

If you can express your algorithm using these patterns, an apparently fundamentally sequential algorithm can be made parallel

Map

- Inputs
  - Array A
  - Function f(x)
- map(A, f) → apply f(x) on all elements in A
- Parallelism trivially exposed
  - f(x) can be applied in parallel to all elements, in principle

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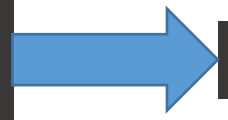
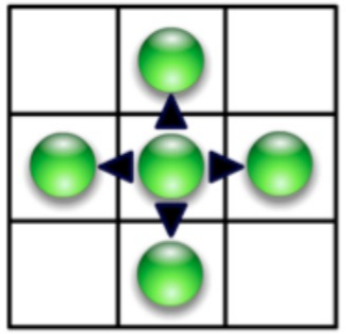
```
for(i=0; i<numPoints; i++) {
   labels[i] = findNearestCenter(points[i]);
}
```



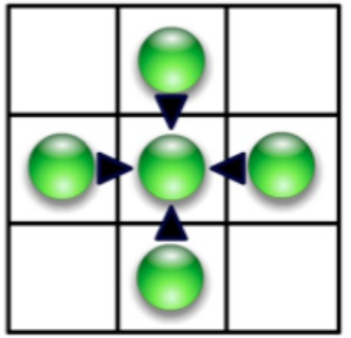
```
map(points, findNearestCenter)
```

Scatter and Gather

- Gather:
  - Read multiple items to single location
- Scatter:
  - Write single data item to multiple locations



Scatter



Gather

Scatter and Gather

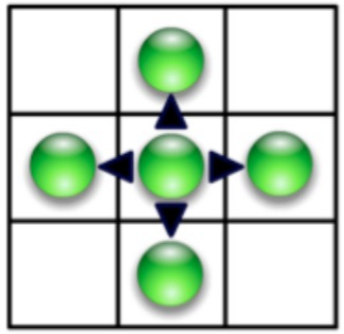
- Gather:
  - Read multiple items to single location
- Scatter:
  - Write single data item to multiple locations

```
for (i=0; i<N; ++i)
  x[i] = y[idx[i]];
```

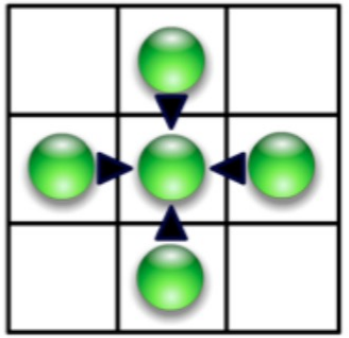
→ gather(x, y, idx)

```
for (i=0; i<N; ++i)
  y[idx[i]] = x[i];
```

→ scatter(x, y, idx)



Scatter



Gather

Reduce

- Input
  - Associative operator op
  - Ordered set s = [a, b, c, … z]
- Reduce(op, s) returns a op b op c … op z

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```
for(i=0; i<N; ++i) {
   accum += (map(sqr, point[i]))
}
```

```
accum = reduce(+, map(sqr, point))
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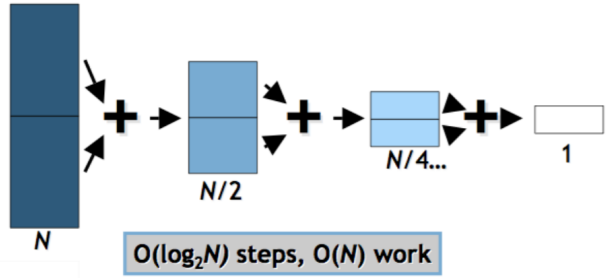

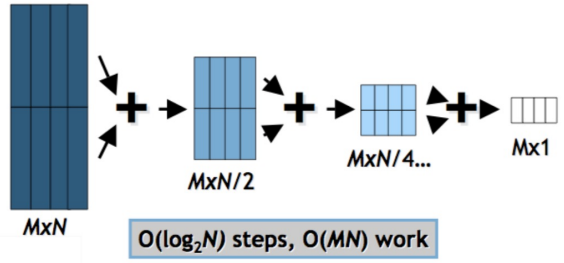


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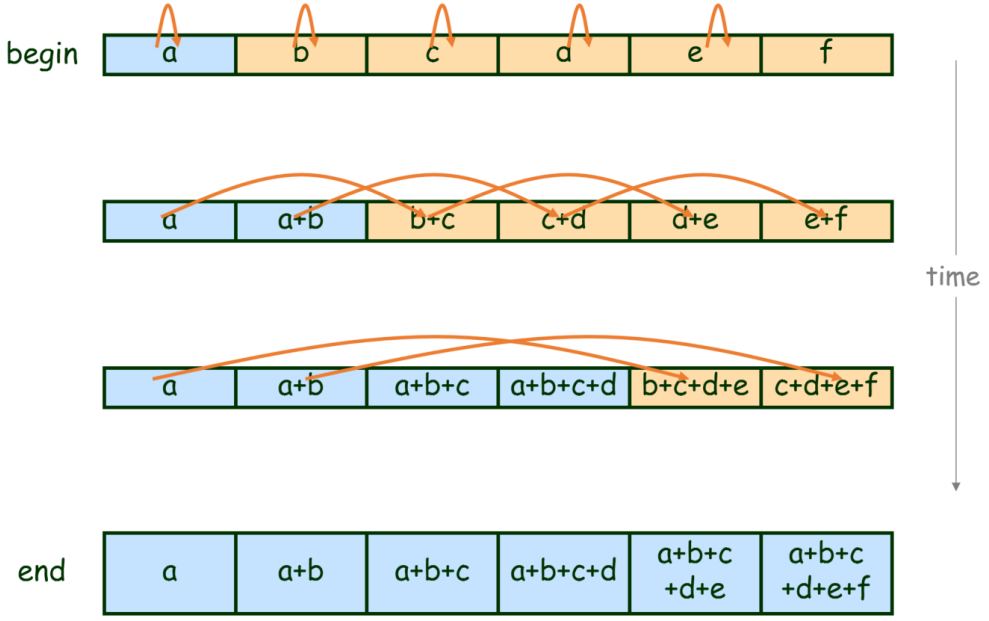
```

Why must op be associative?

Scan (prefix sum)

- Input
  - Associative operator op
  - Ordered set s = [a, b, c, … z]
  - Identity I
- scan(op, s) = [I, a, (a op b), (a op b op c) …]
- Scan is the workhorse of parallel algorithms:
  - Sort, histograms, sparse matrix, string compare, …



Summary

- Re-expressing apparently sequential algorithms as combinations of parallel patterns is a common technique when targeting GPUs