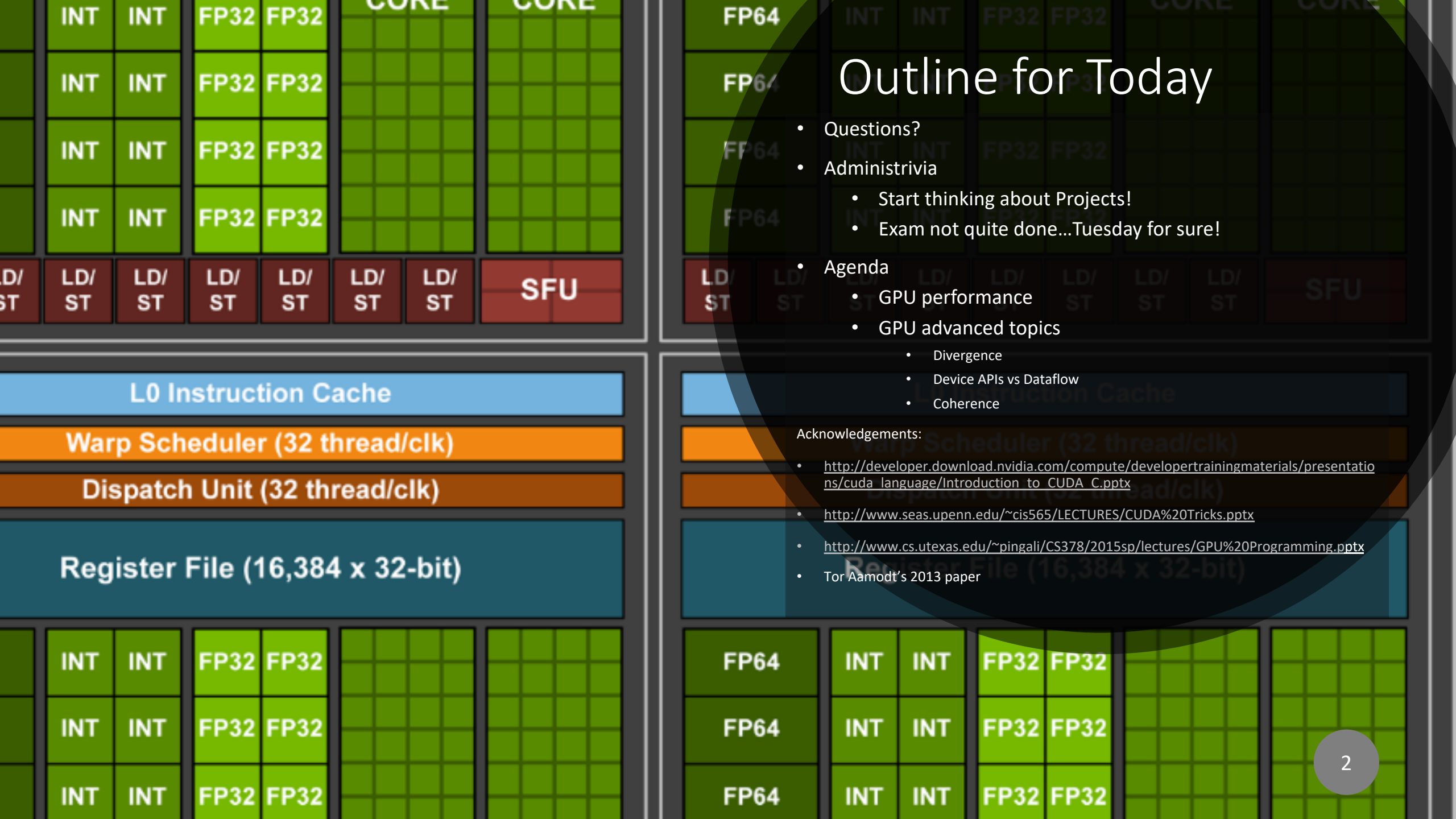
GPUs going once…
GPUs going twice…
you get the idea

Chris Rossbach

cs378



Outline for Today

- Questions?
- Administrivia
  - Start thinking about Projects!
  - Exam not quite done…Tuesday for sure!
- Agenda
  - GPU performance
  - GPU advanced topics
    - Divergence
    - Device APIs vs Dataflow
    - Coherence

Acknowledgements:

- http://developer.download.nvidia.com/compute/developertrainingmaterials/presentations/cuda_language/Introduction_to_CUDA_C.pptx
- http://www.seas.upenn.edu/~cis565/LECTURES/CUDA%20Tricks.pptx
- http://www.cs.utexas.edu/~pingali/CS378/2015sp/lectures/GPU%20Programming.pptx
- Tor Aamodt's 2013 paper

Faux Quiz Questions

- How is occupancy defined (in CUDA nomenclature)?
- What's the difference between a block scheduler (e.g. Giga-Thread Engine) and a warp scheduler?
- Modern CUDA supports UVM to eliminate the need for cudaMalloc and cudaMemcpy*. Under what conditions might you want to use or not use it and why?
- What is control flow divergence? How does it impact performance?
- What is a bank conflict?
- What is work efficiency?
- What is the difference between a thread block scheduler and a warp scheduler?
- How are atomics implemented in modern GPU hardware?
- How is __shared__ memory implemented by modern GPU hardware?
- Why is __shared__ memory necessary if GPUs have an L1 cache? When will an L1 cache provide all the benefit of __shared__ memory and when will it not?
- Is cudaDeviceSynchronize still necessary after copyback if I have just one CUDA stream?

How many threads/blocks?

```
    // Copy inputs to device
    cudaMemcpy(d_a, a, size, cudaMemcpyHostToDevice);
    cudaMemcpy(d_b, b, size, cudaMemcpyHostToDevice);

    // Launch add() kernel on GPU
    add<<<N/THREADS_PER_BLOCK, THREADS_PER_BLOCK>>>(d_a, d_b, d_c);

    // Copy result back to host
    cudaMemcpy(c, d_c, size, cudaMemcpyDeviceToHost);

    // Cleanup
    free(a); free(b); free(c);
    cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);
    return 0;
}
```

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- Usually things are correct if grid*block dims >= input size
- Getting good performance is another matter

Review: Internals

```
__host__
void vecAdd()
{
  dim3 DimGrid = (ceil(n/256,1,1);
  dim3 DimBlock = (256,1,1);
  addKernel<<<DGrid,DBlock>>>(A_d,B_d,C_d,n);
}
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__global__
void addKernel(float *A_d,
               float *B_d,
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   int i = blockIdx.x * blockDim.x
           + threadIdx.x;
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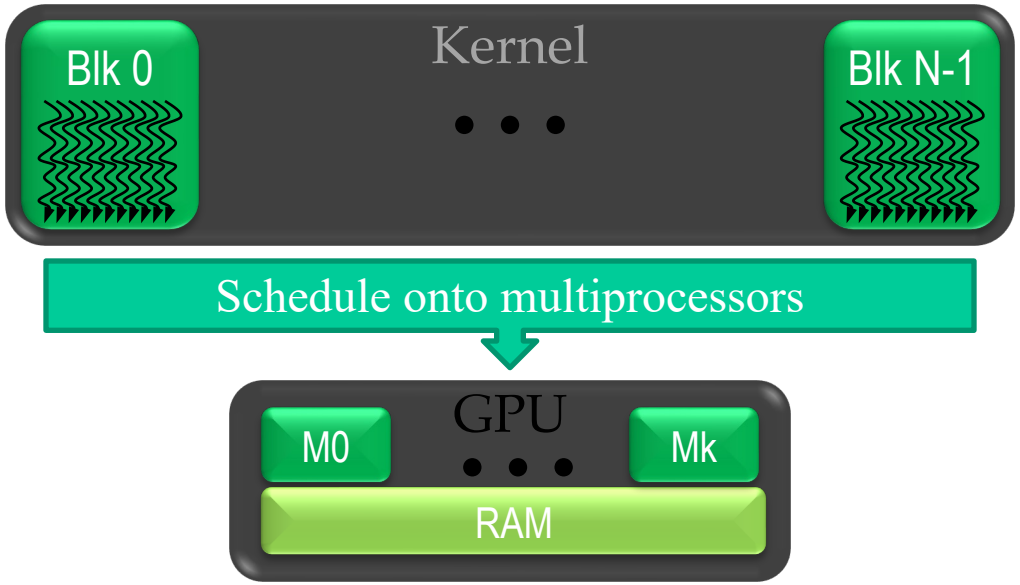

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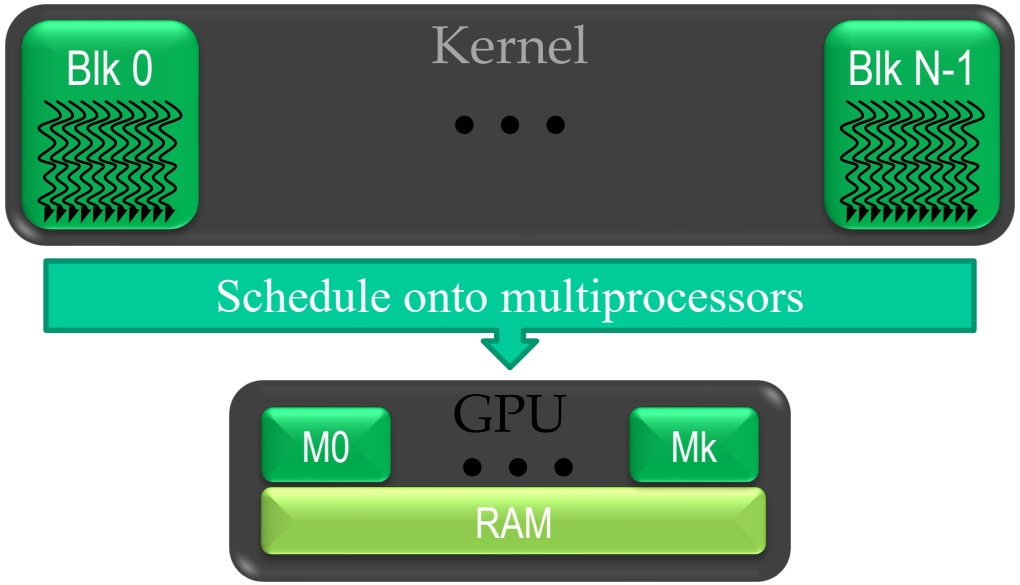

How are threads scheduled?

Thread Blocks, Warps, Scheduling

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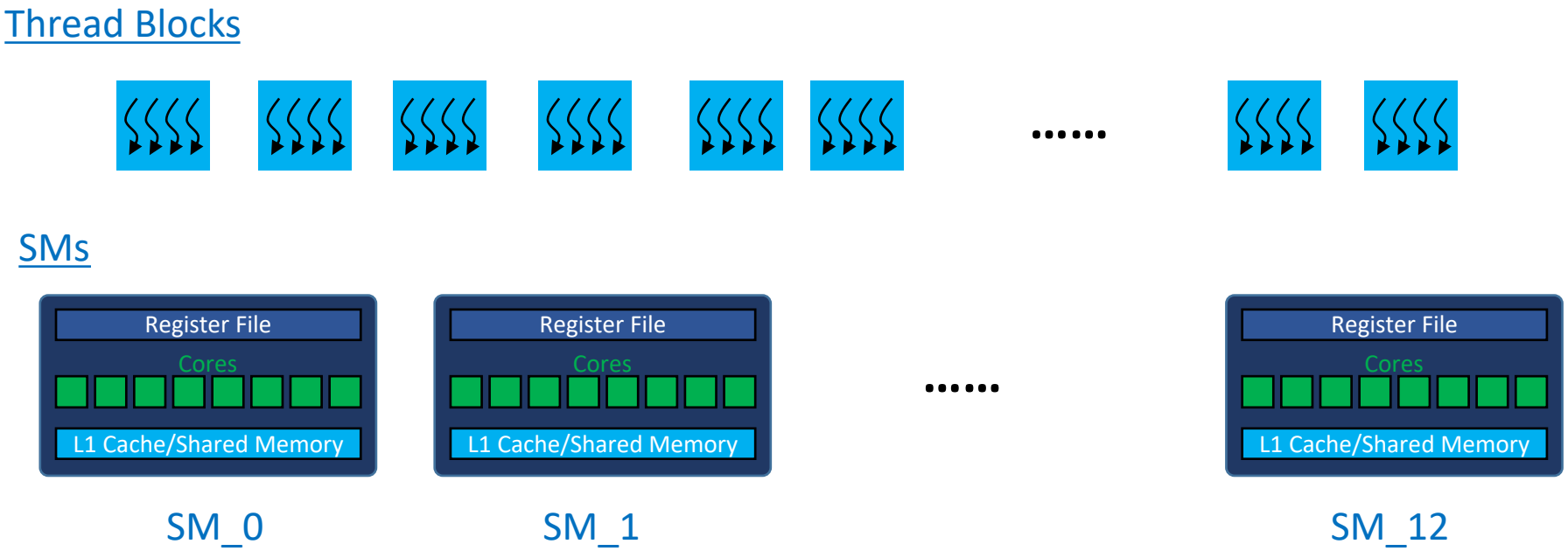

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- 32 threads each

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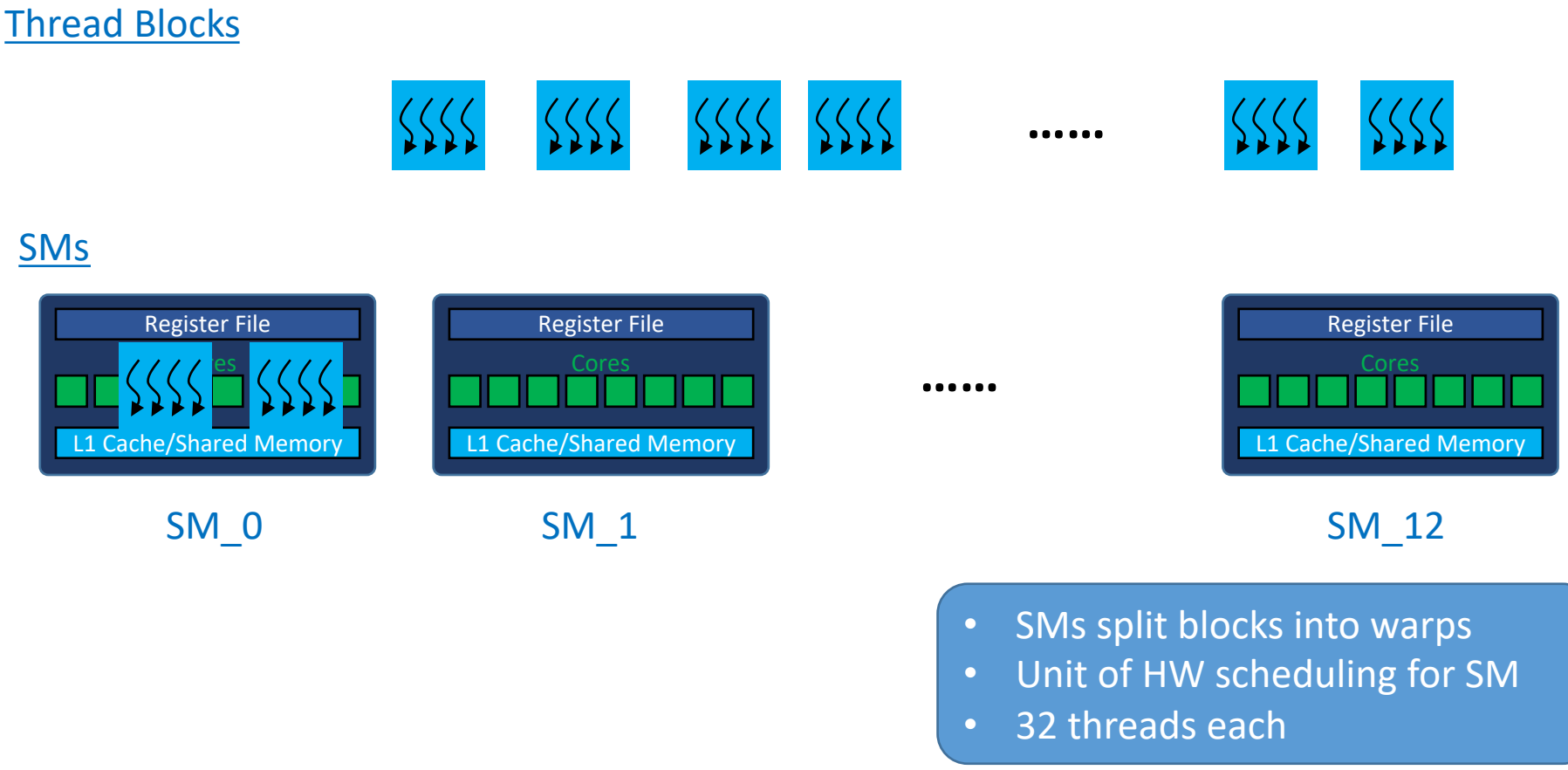

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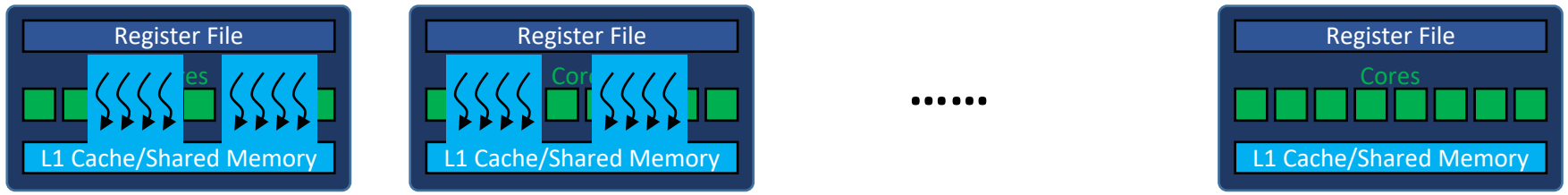

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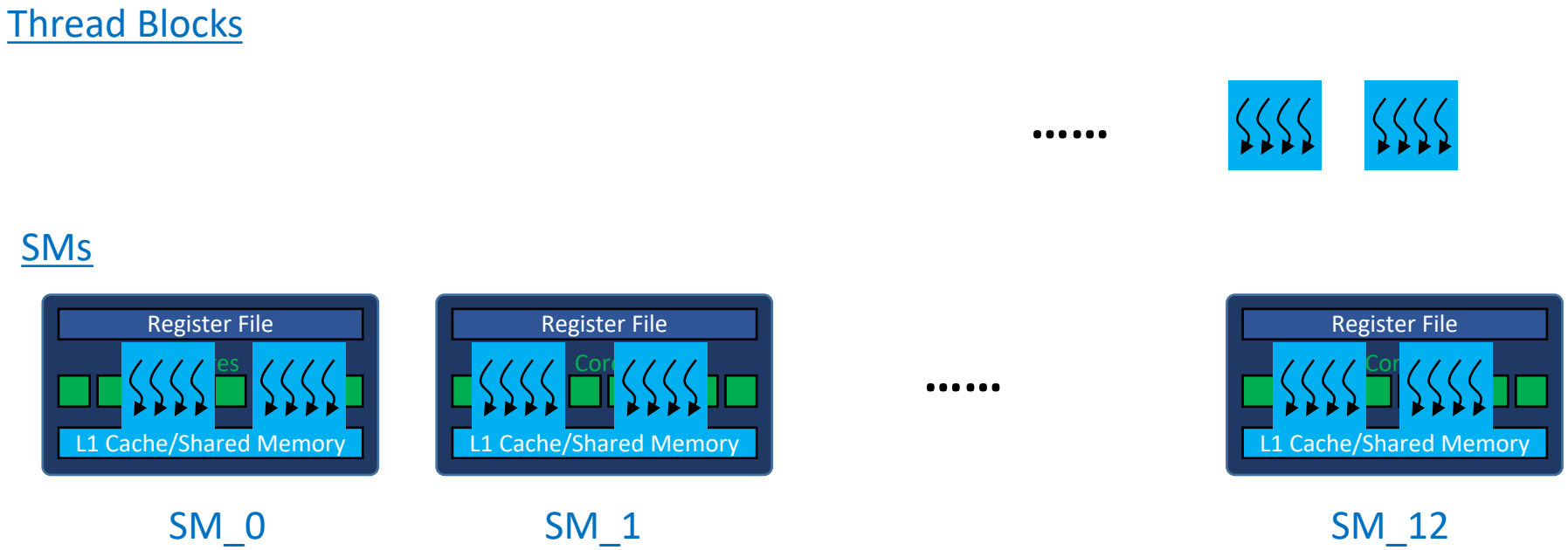

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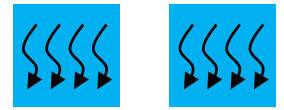
Thread Blocks

Remaining TBs are queued



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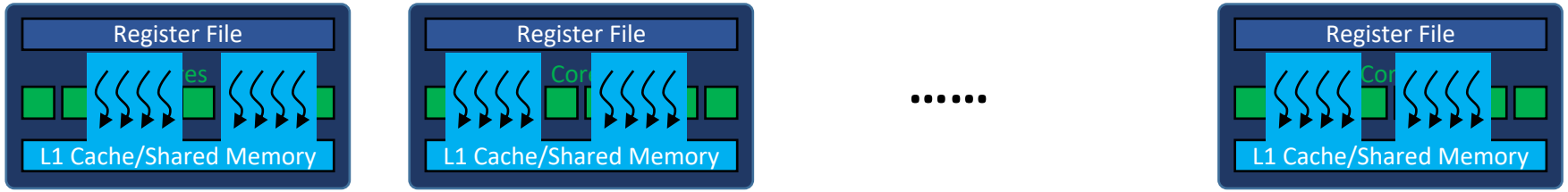

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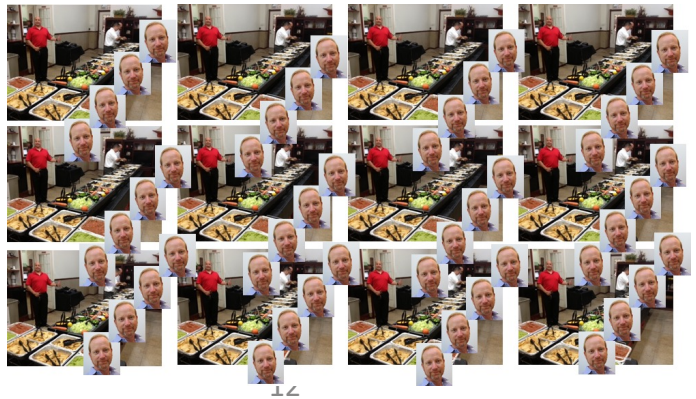

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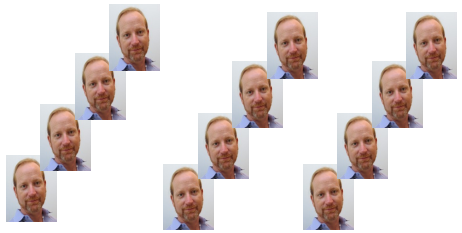

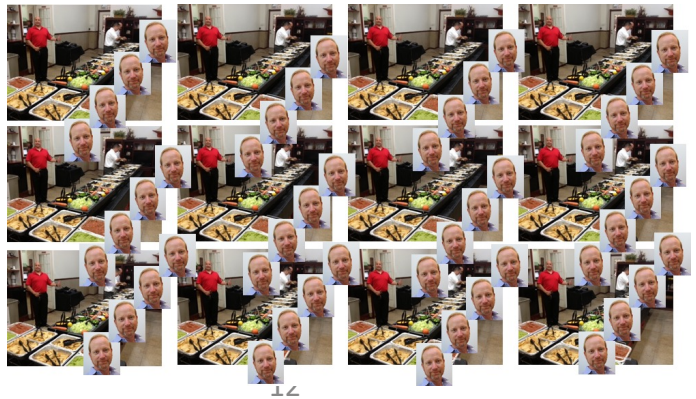

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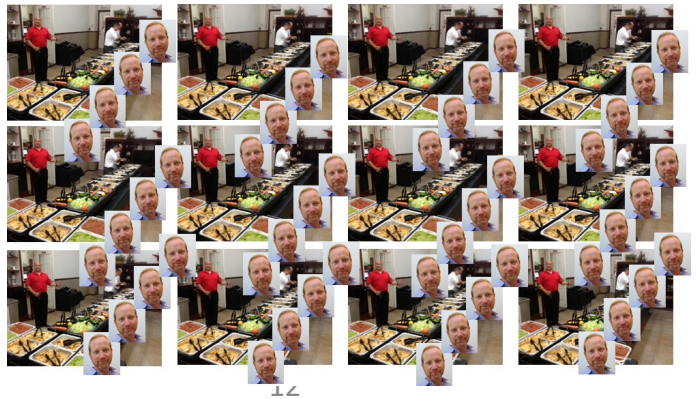

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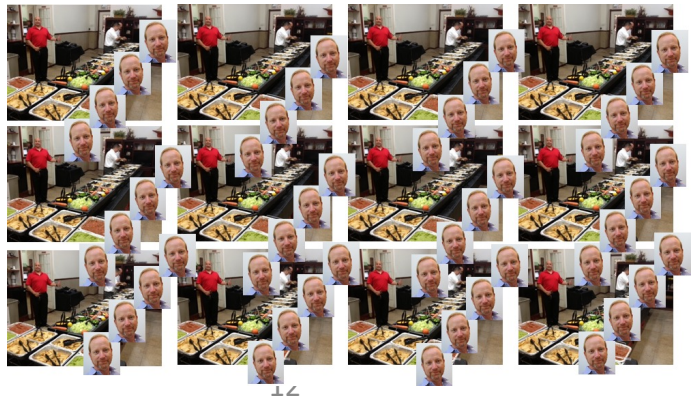

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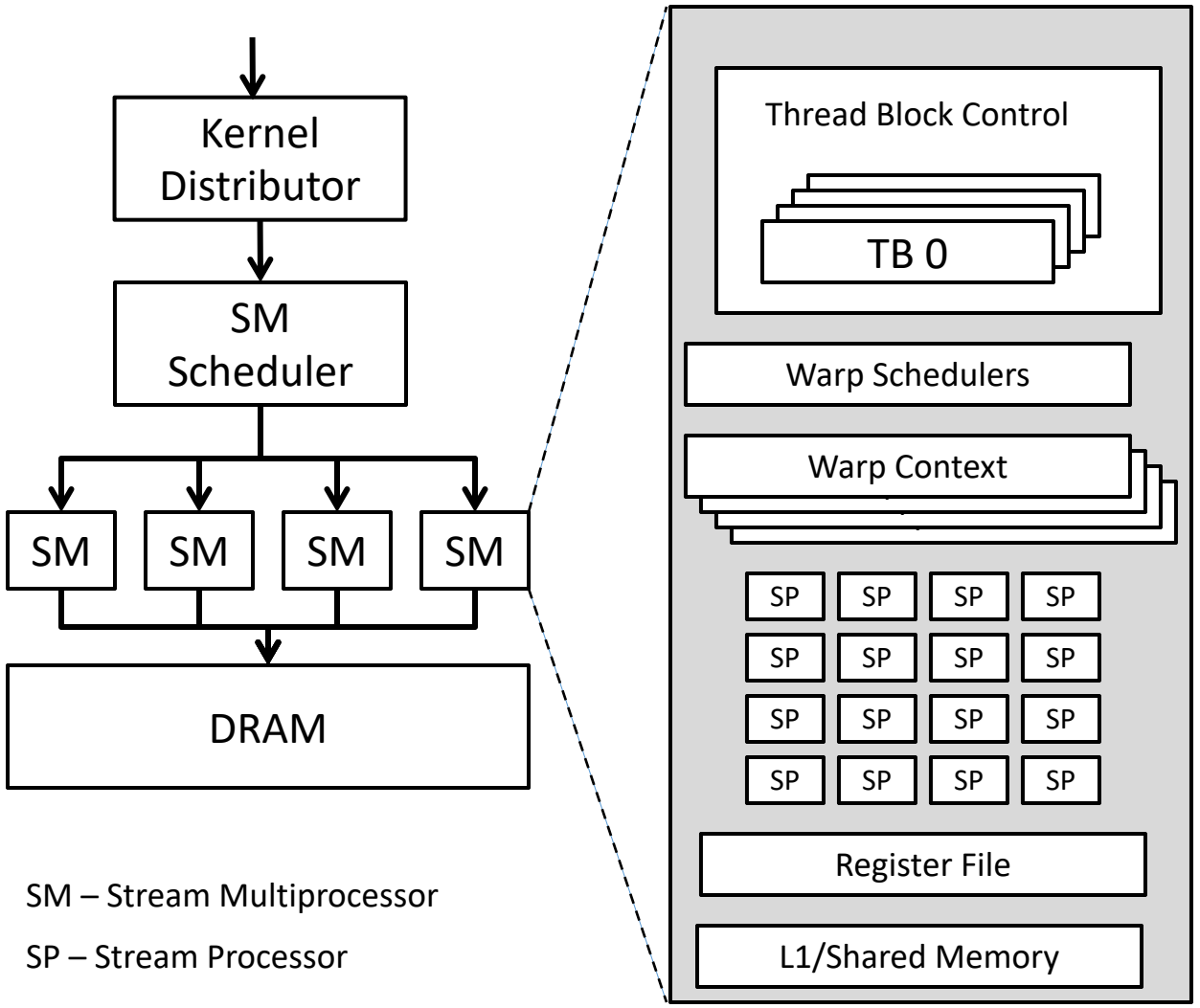

SM – Stream Multiprocessor

SP – Stream Processor

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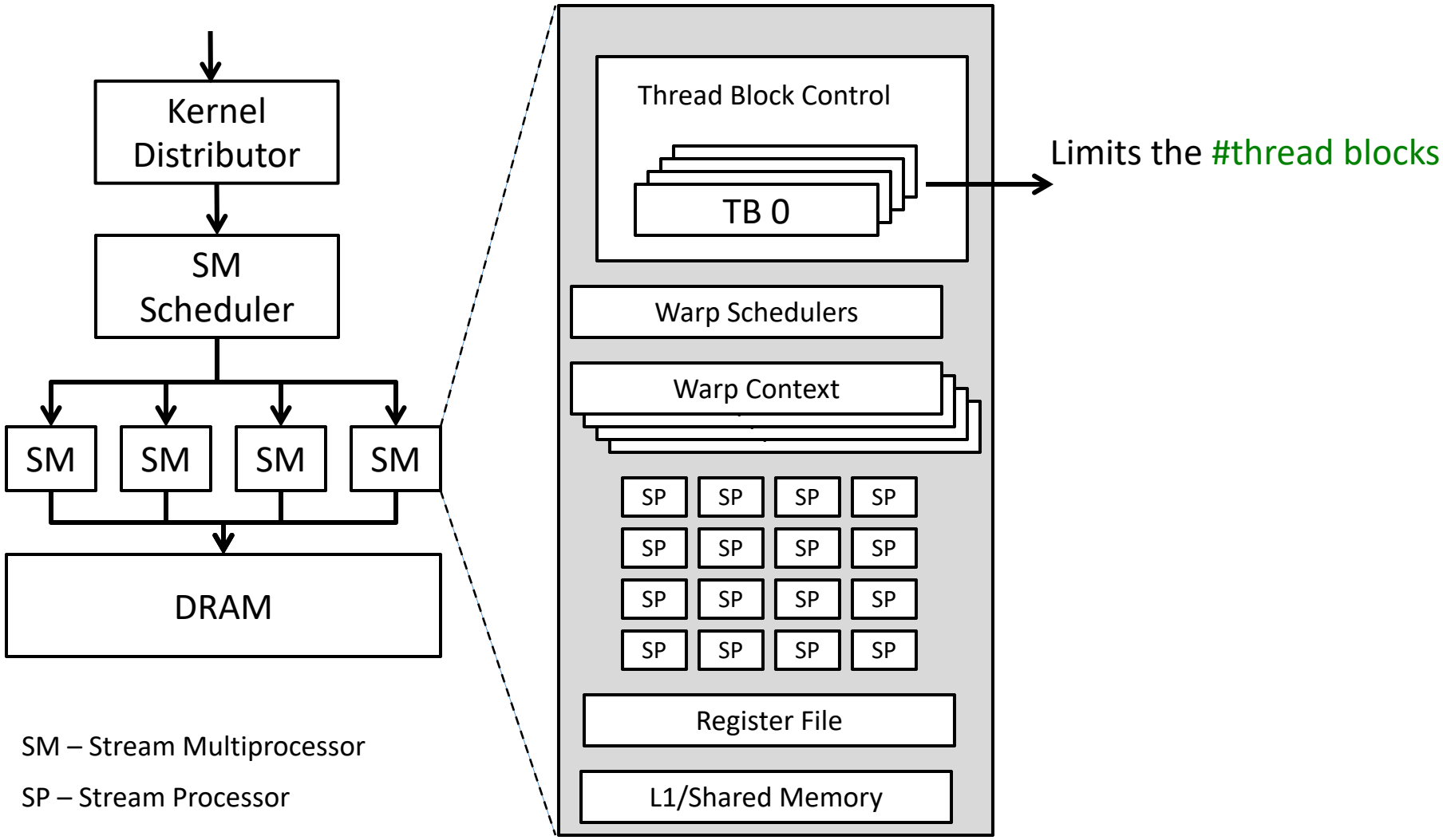

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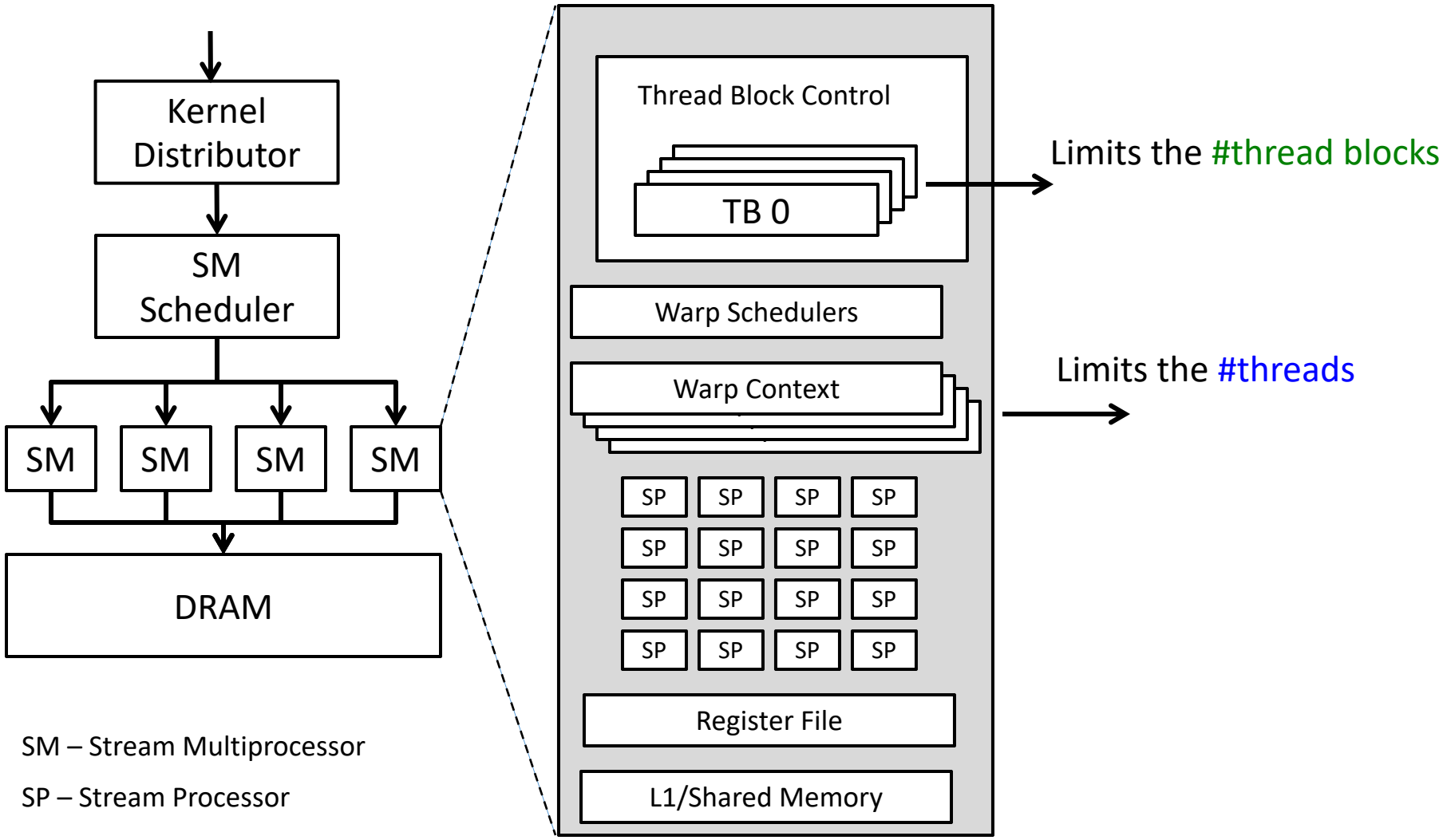

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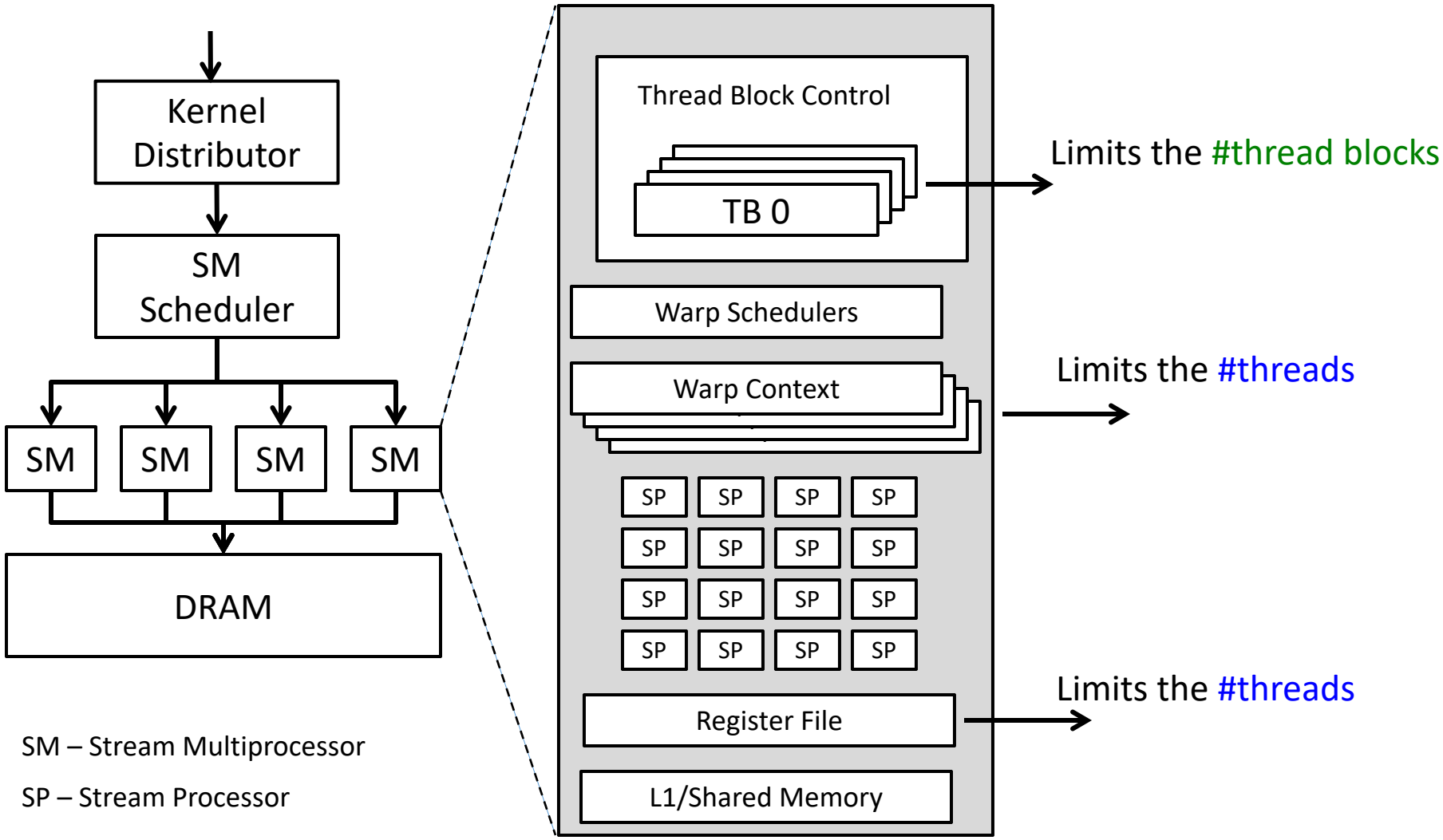

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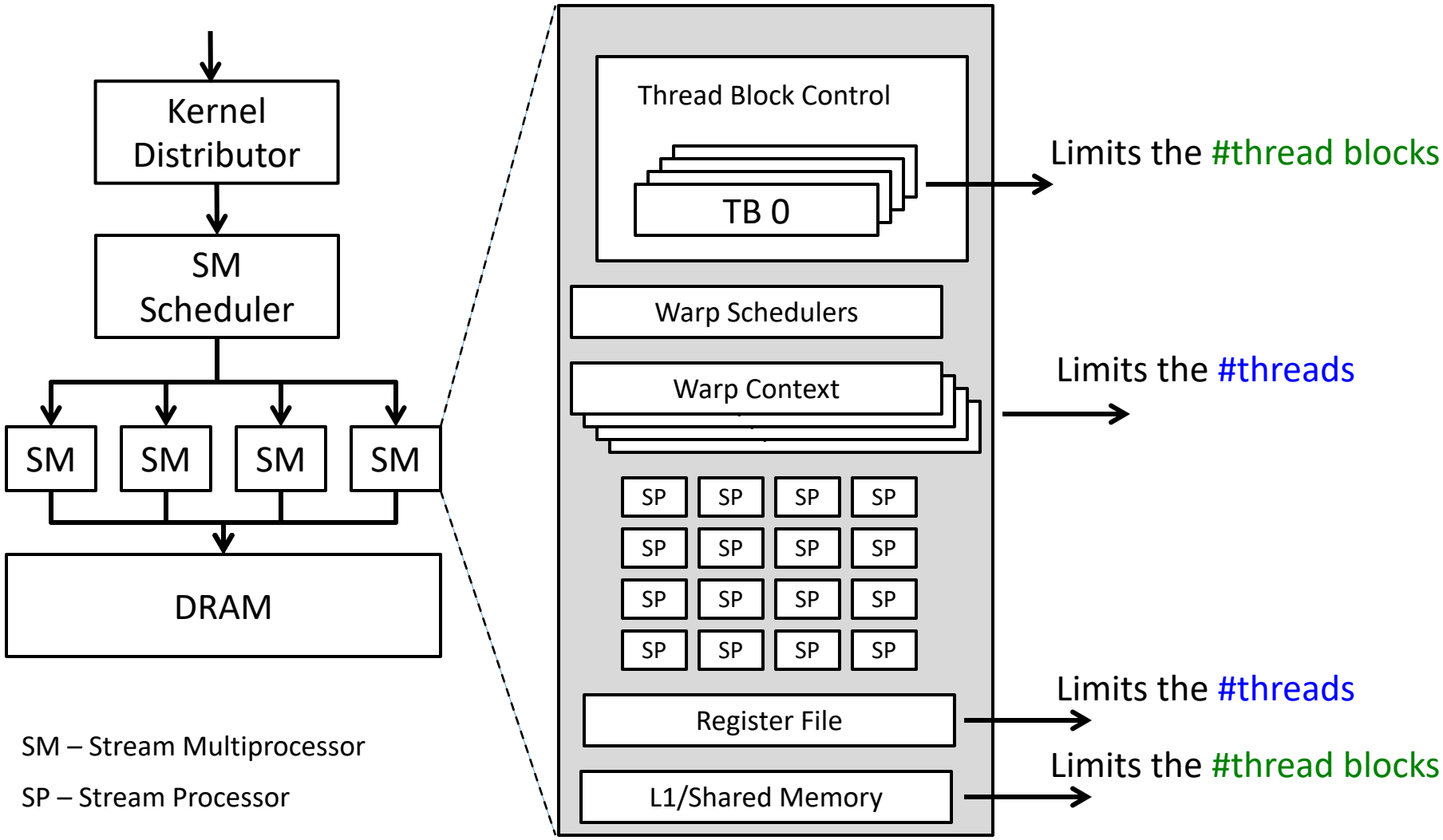

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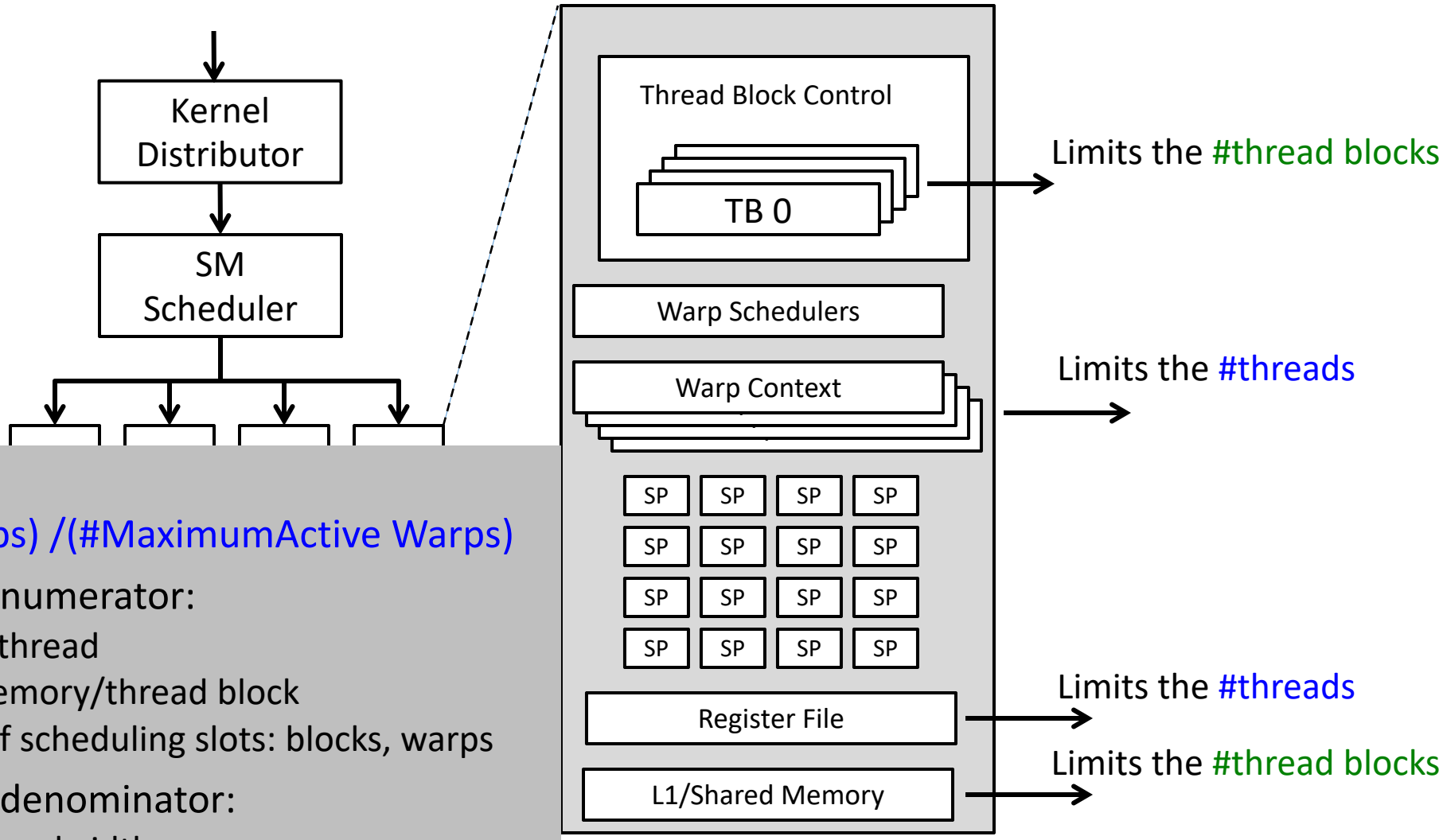

Occupancy:

- (#Active Warps) /(#MaximumActive Warps)
- Limits on the numerator:
  - Registers/thread
  - Shared memory/thread block
  - Number of scheduling slots: blocks, warps
- Limits on the denominator:
  - Memory bandwidth
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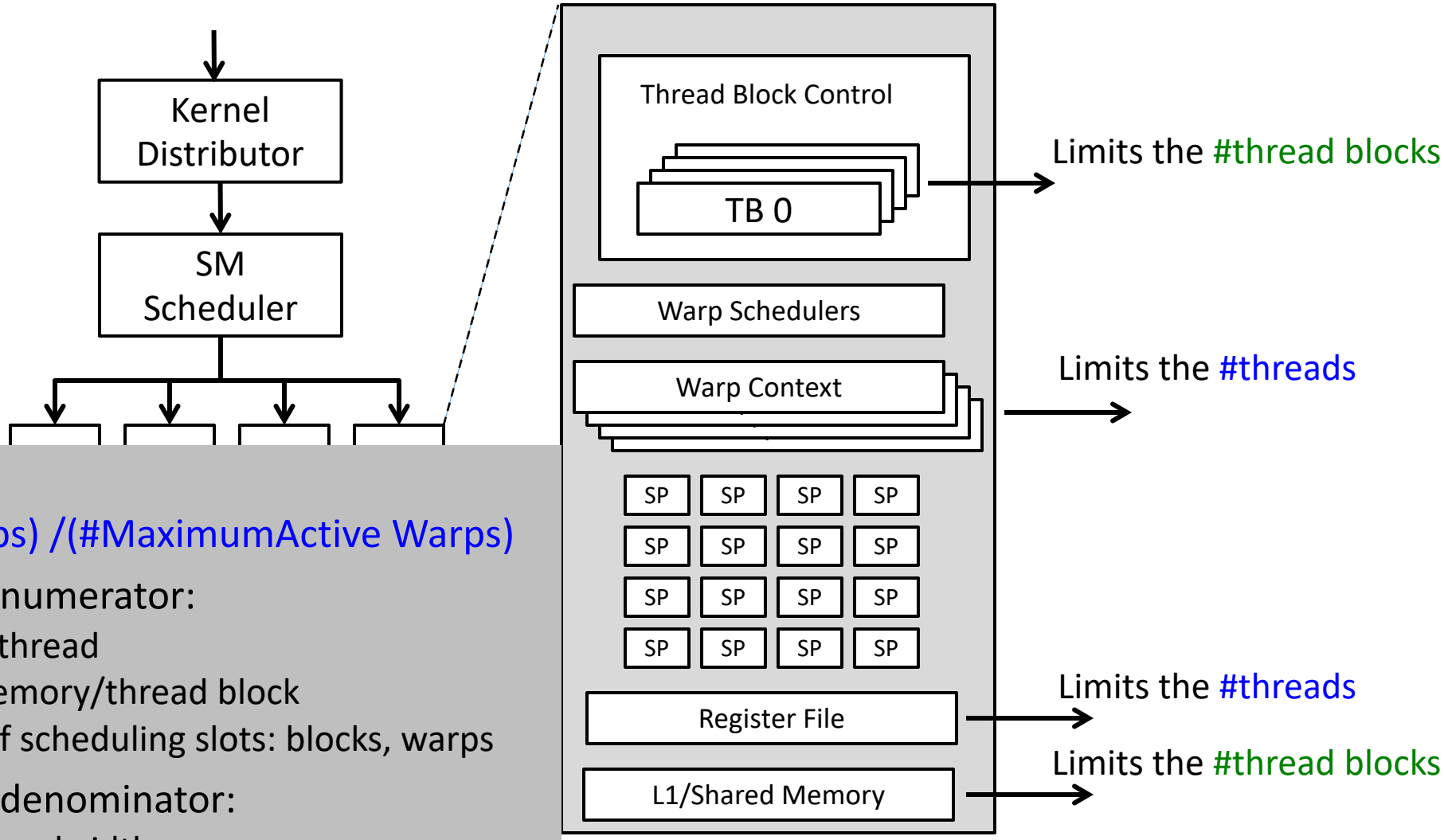

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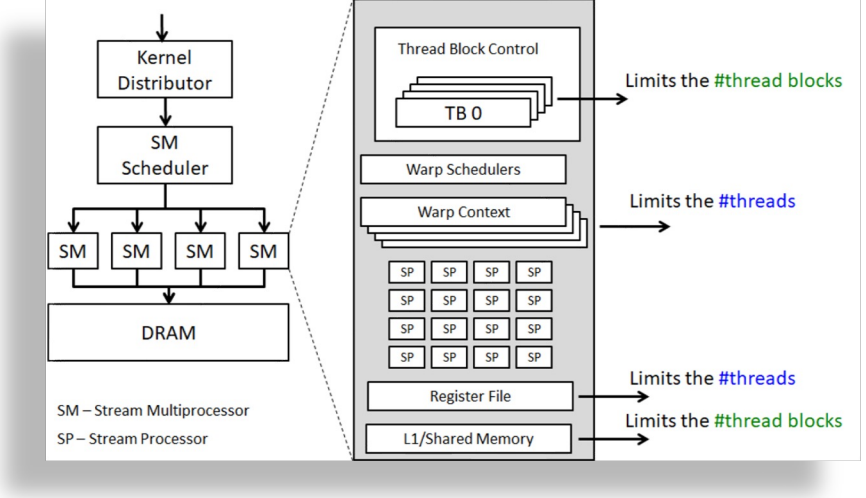
What is the performance impact of varying kernel resource demands?

Impact of Thread Block Size



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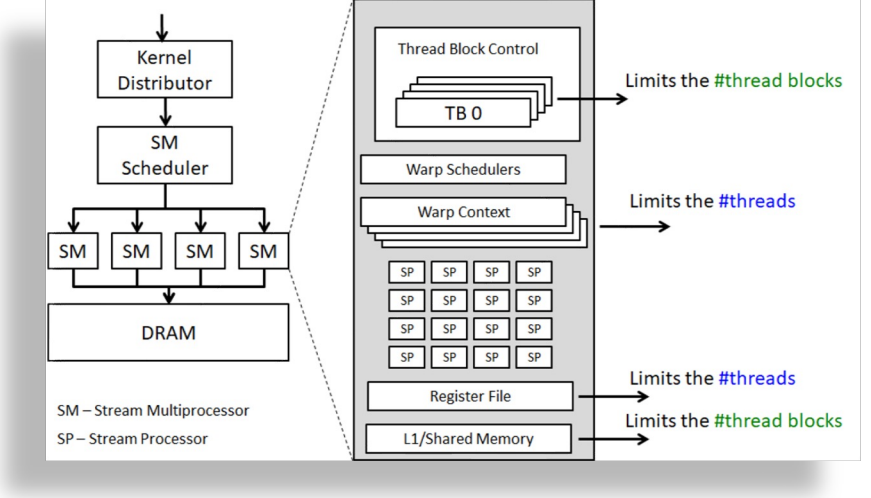

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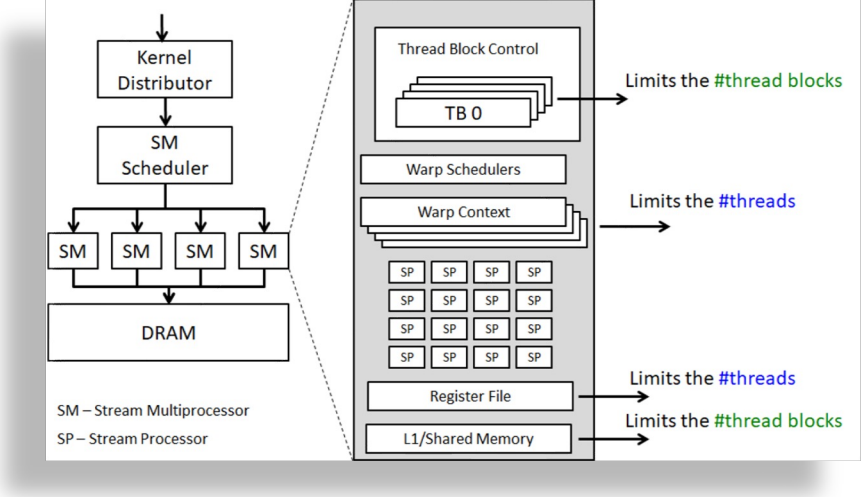

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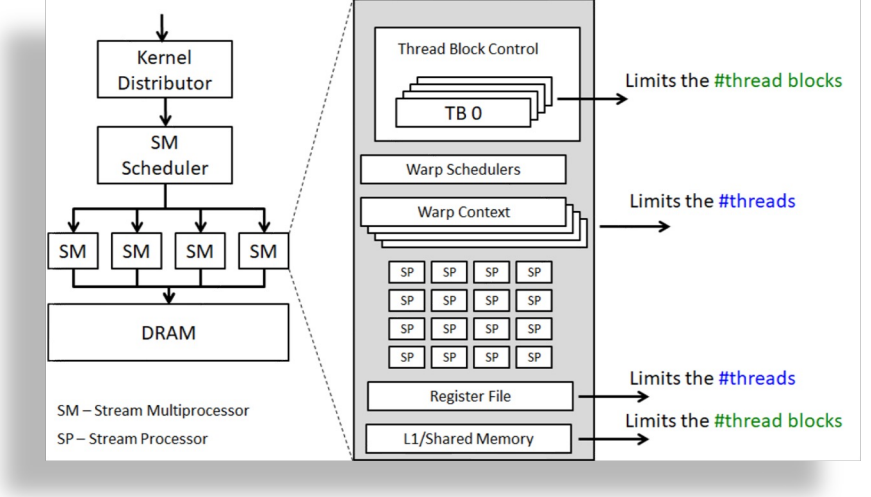

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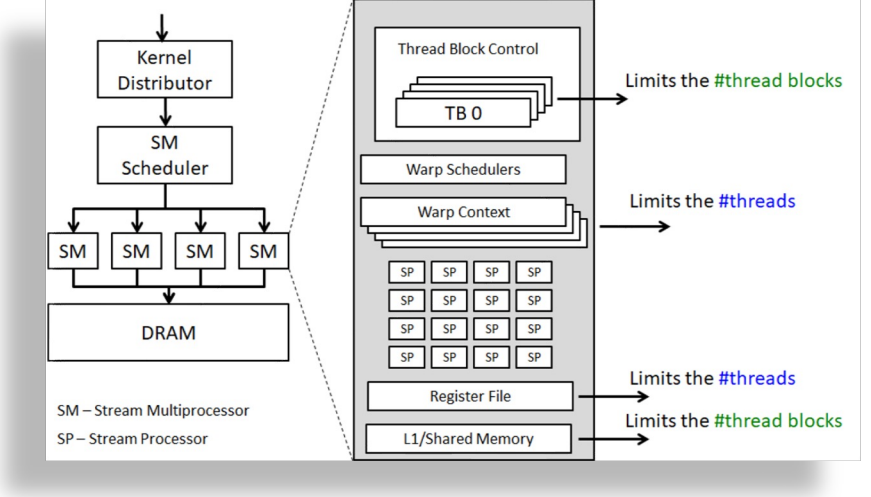

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- max active warps/SM == 64 (limit: warp context)
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  - With 512 threads/block how many blocks can execute (per SM) concurrently?
  - Max active warps * threads/warp = 64*32 = 2048 threads →

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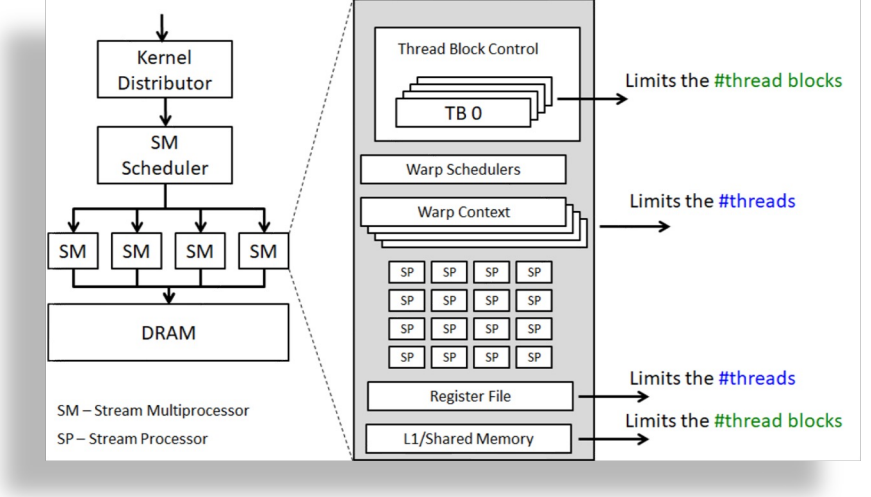

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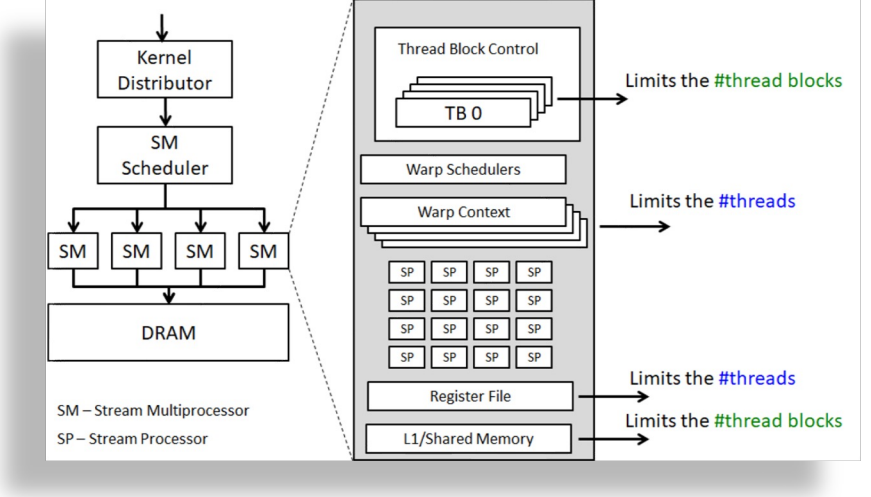

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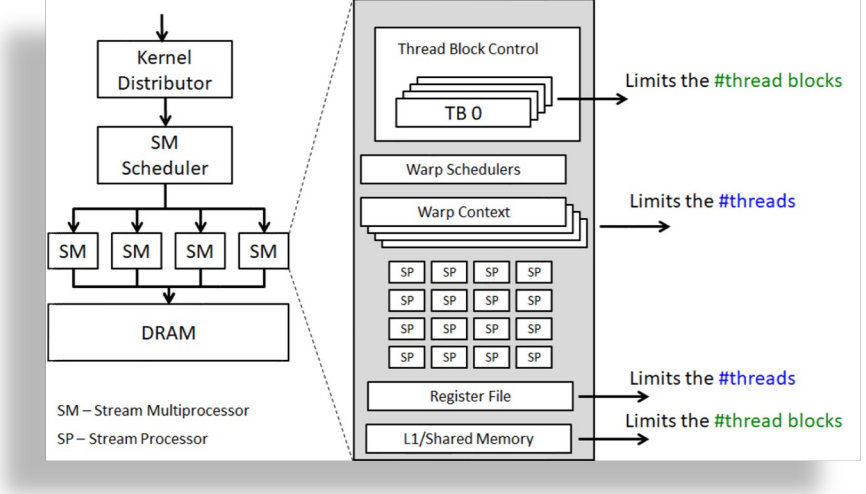

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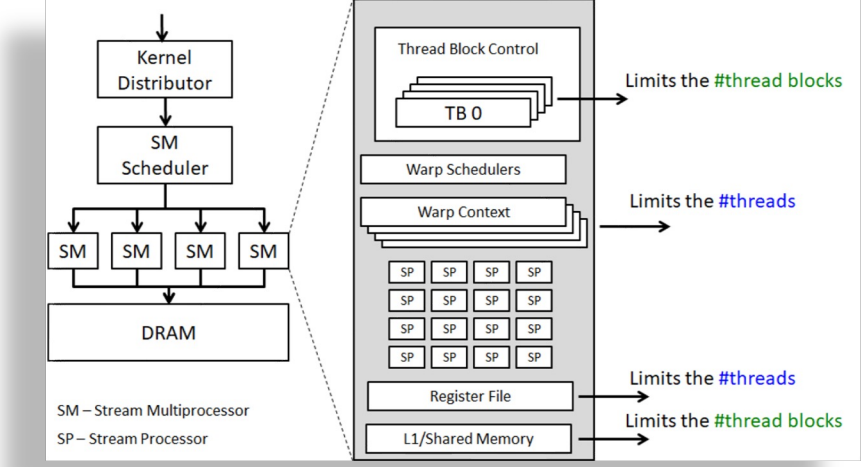

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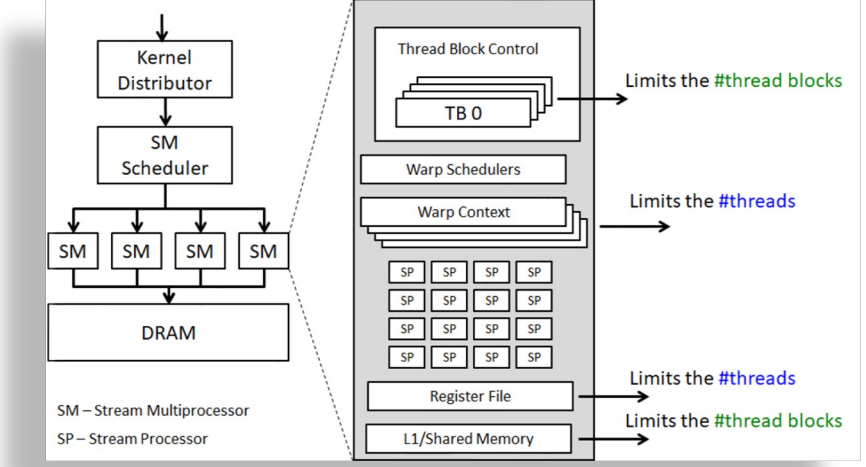

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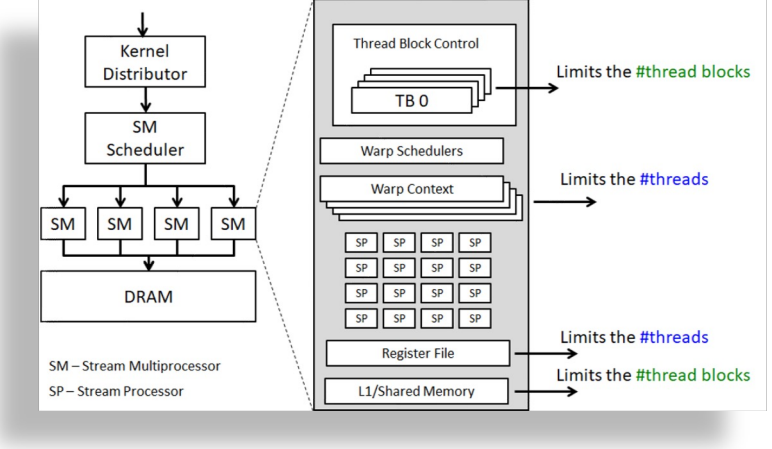
  - Blocks are maxed out, but max active threads = 32*32 = 1024
  - Occupancy = .5 (1024/2048)
- To maximize utilization, thread block size should balance
  - Limits on active thread blocks vs.
  - Limits on active warps

Impact of #Registers Per Thread



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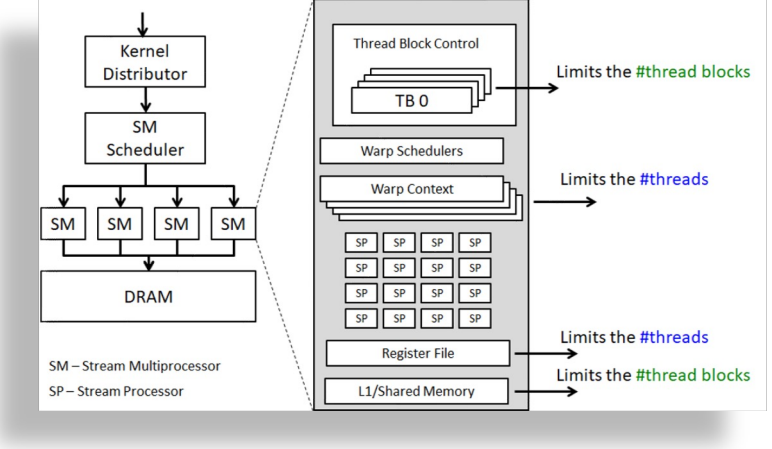

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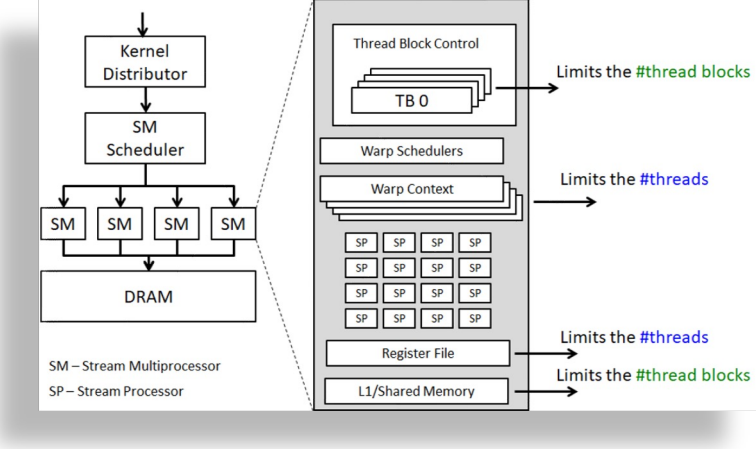

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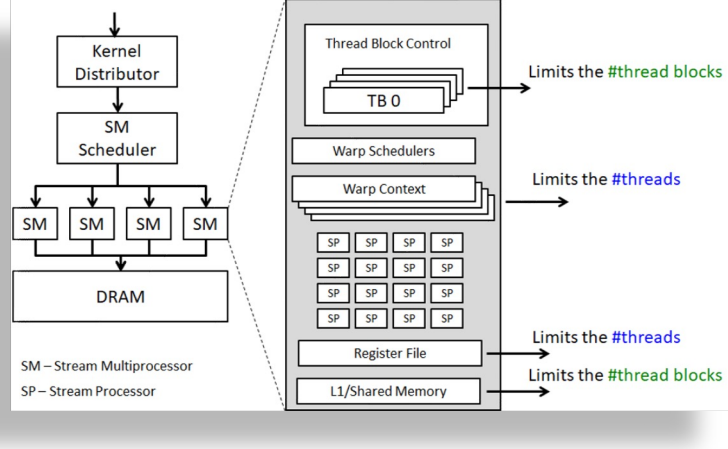

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V100:

- Registers per thread max: 255

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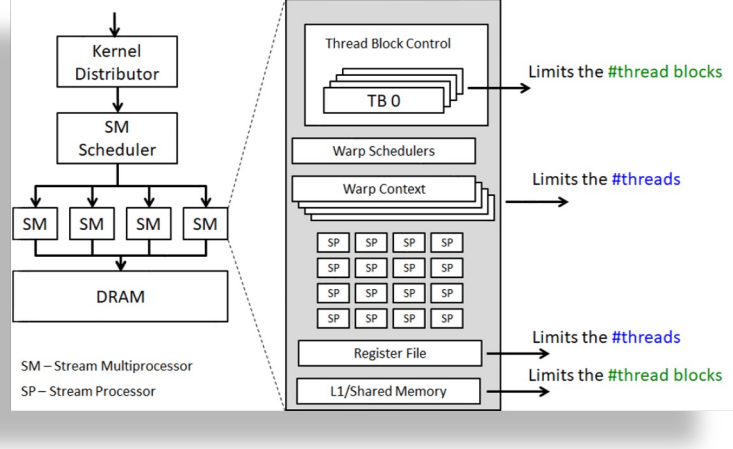

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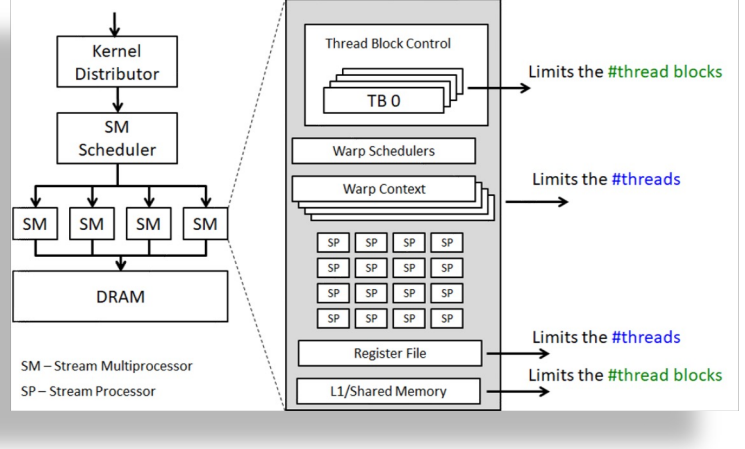

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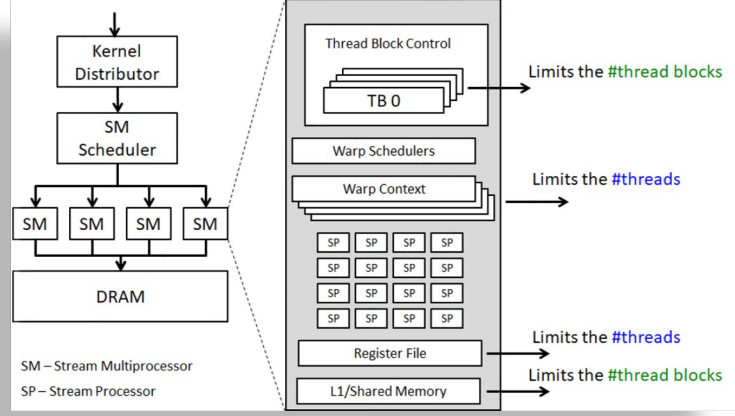

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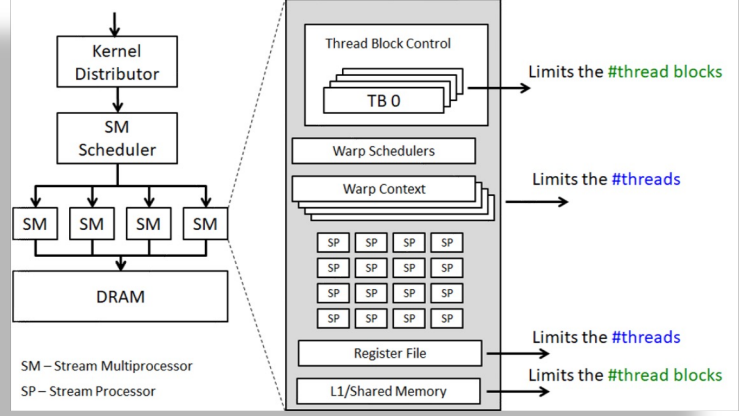

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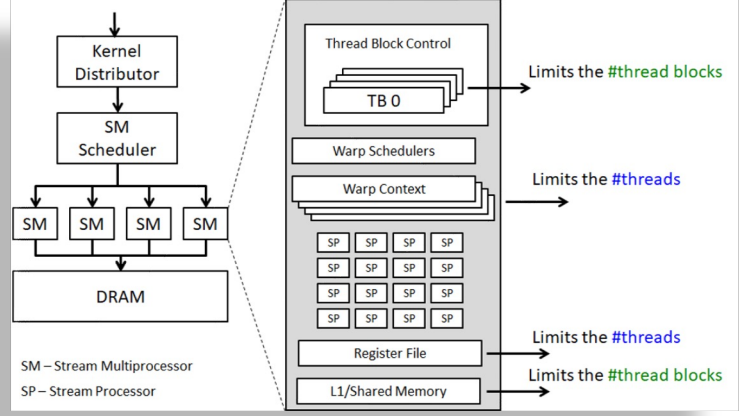

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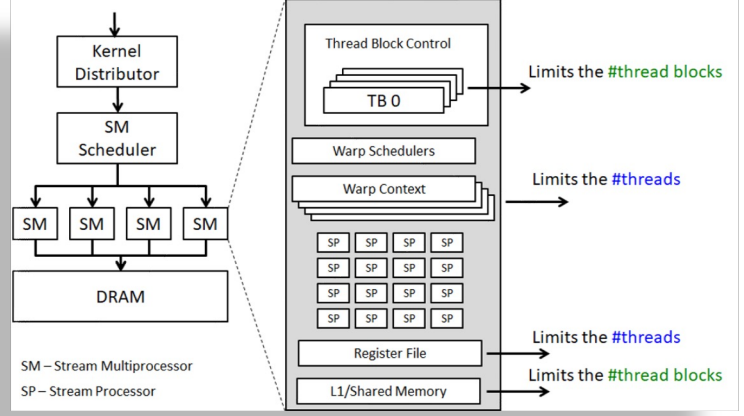

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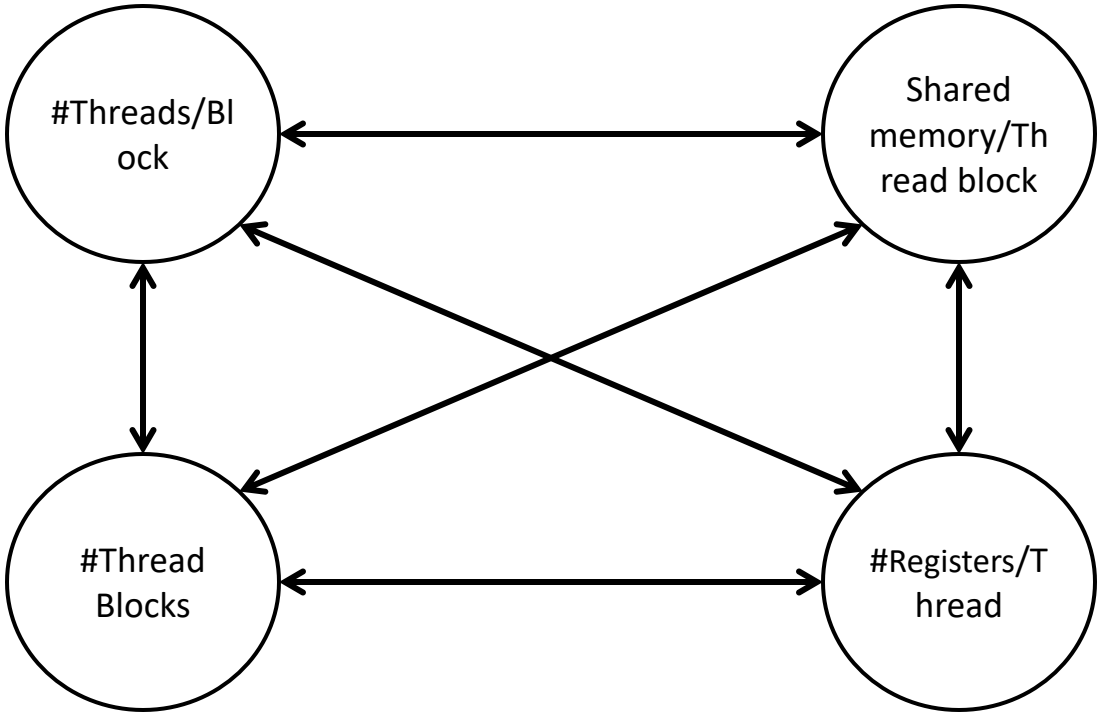
  - *FULLY Occupied!*
- What is the impact of increasing number of registers by 2?
  - Recall: granularity of management is a thread block!
  - Loss of concurrency of 256 threads!
  - *34 regs/thread * 256 threads/block * 7 blocks/SM = 60k registers,*
  - *8 blocks would over-subscribe register file*
  - *Occupancy drops to .875!*

Impact of Shared Memory

- Shared memory is allocated per thread block
  - Can limit the number of thread blocks executing concurrently per SM
  - Shared mem/block * # blocks <= total shared mem per SM
- gridDim and blockDim parameters impact demand for
  - shared memory
  - number of thread slots
  - number of thread block slots

Balance



- Navigate the tradeoffs
  - maximize core utilization and memory bandwidth utilization
  - Device-specific
- Goal: Increase occupancy until one or the other is saturated

Balance

```
template < class T >
__host__ cudaError_t cudaOccupancyMaxActiveBlocksPerMultiprocessor ( int* numBlocks, T func, int  blockSize, size_t dynamicSMemSize ) [inline]
```

Returns occupancy for a device function.

Parameters

`numBlocks`
- Returned occupancy

`func`
- Kernel function for which occupancy is calulated

`blockSize`
- Block size the kernel is intended to be launched with

`dynamicSMemSize`
- Per-block dynamic shared memory usage intended, in bytes

- Navigate the tradeoffs
  - maximize core utilization and memory bandwidth utilization
  - Device-specific
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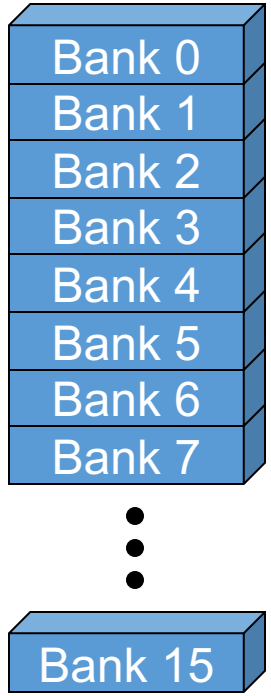
Parallel Memory Accesses

- Coalesced main memory access (16/32x faster)
  - HW combines multiple warp memory accesses into a single coalesced access
- Bank-conflict-free shared memory access (16/32)
  - No alignment or contiguity requirements
    - CC 2.x+3.0 : 32 different banks + 1-word broadcast each

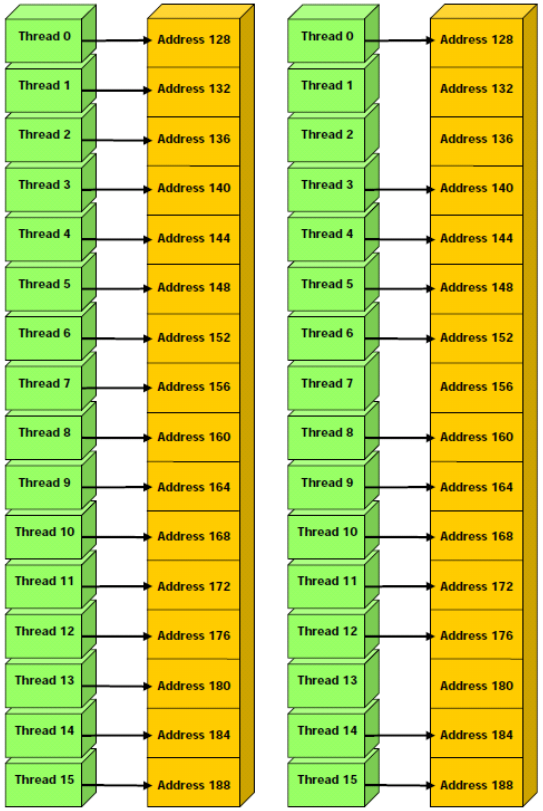
Parallel Memory Architecture

- In a parallel machine, many threads access memory
  - Therefore, memory is divided into banks
  - Essential to achieve high bandwidth
- Each bank can service one address per cycle
  - A memory can service as many simultaneous accesses as it has banks
- Multiple simultaneous accesses to a bank result in a bank conflict
  - Conflicting accesses are serialized



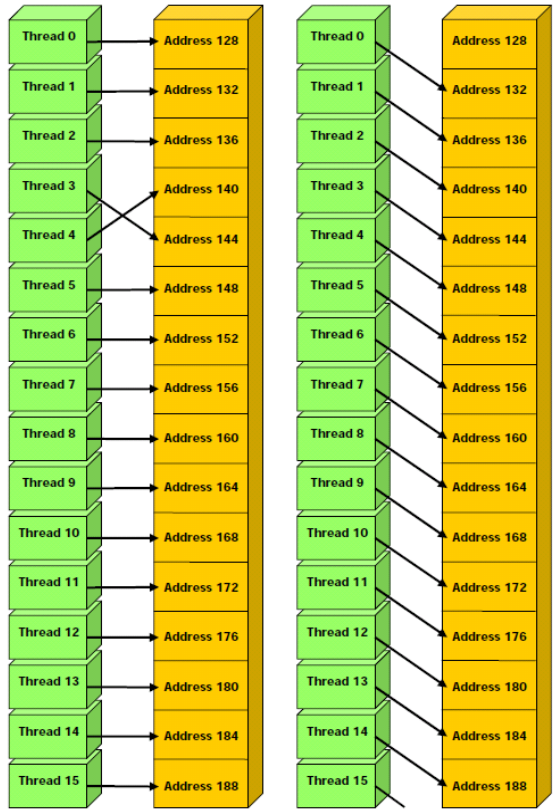
Coalesced Main Memory Accesses

single coalesced access



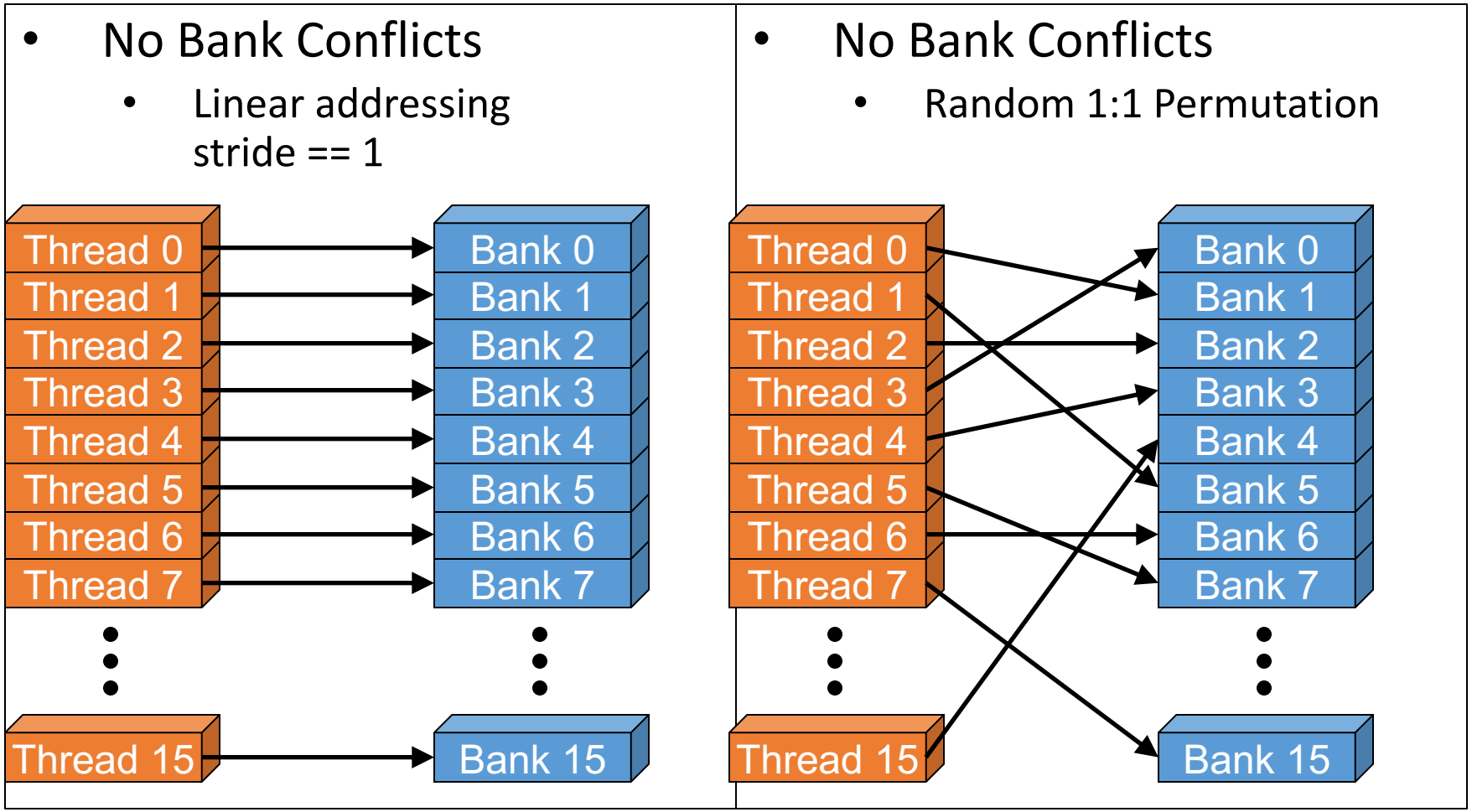
NVIDIA

one and two coalesced accesses*



NVIDIA

Bank Addressing Examples



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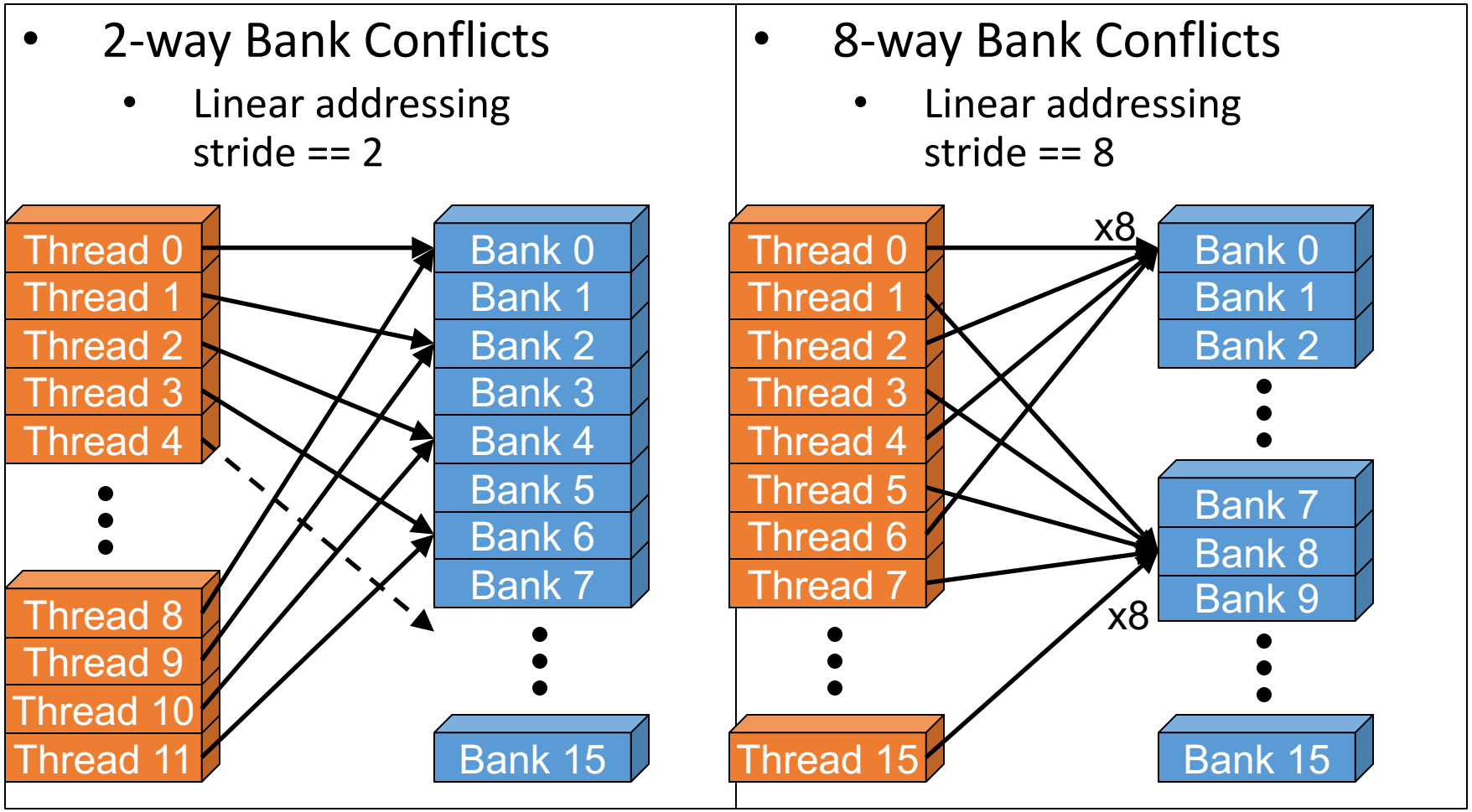
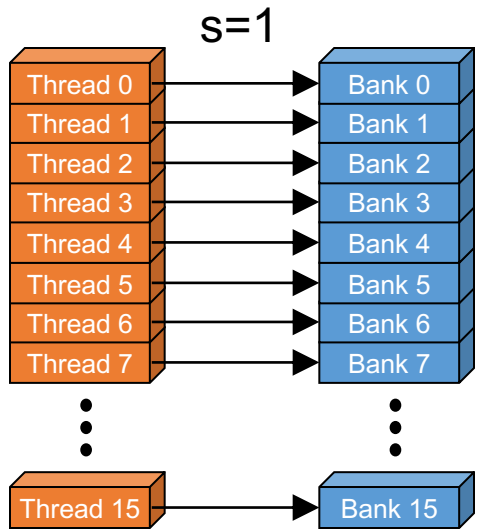


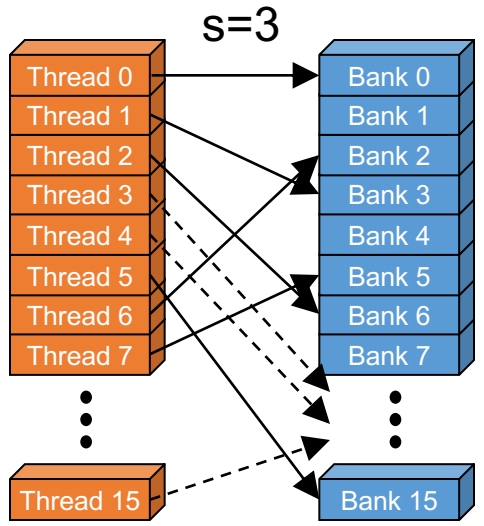
Linear Addressing

- Given:

```
__shared__ float shared[256];
float foo =
    shared[baseIndex + s *
     threadIdx.x];
```



- This is only bank-conflict-free if s shares no common factors with the number of banks
  - 16 on G80, so `s` must be odd



GPU Atomics & Divergence

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Race conditions –

- Traditional locks: avoid!
- How do we synchronize?

Read-Modify-Write – atomic

```
atomicAdd()          atomicInc()
atomicSub()          atomicDec()
atomicMin()          atomicExch()
atomicMax()          atomicCAS()
```

Implemented as write-through to L2

- “Fire-and-forget”

GPU Atomics & Diverg

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// Add "val" to "*data". Return old value.
double atomicAdd(double *data, double val)
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    while(atomicExch(&locked, 1) != 0)
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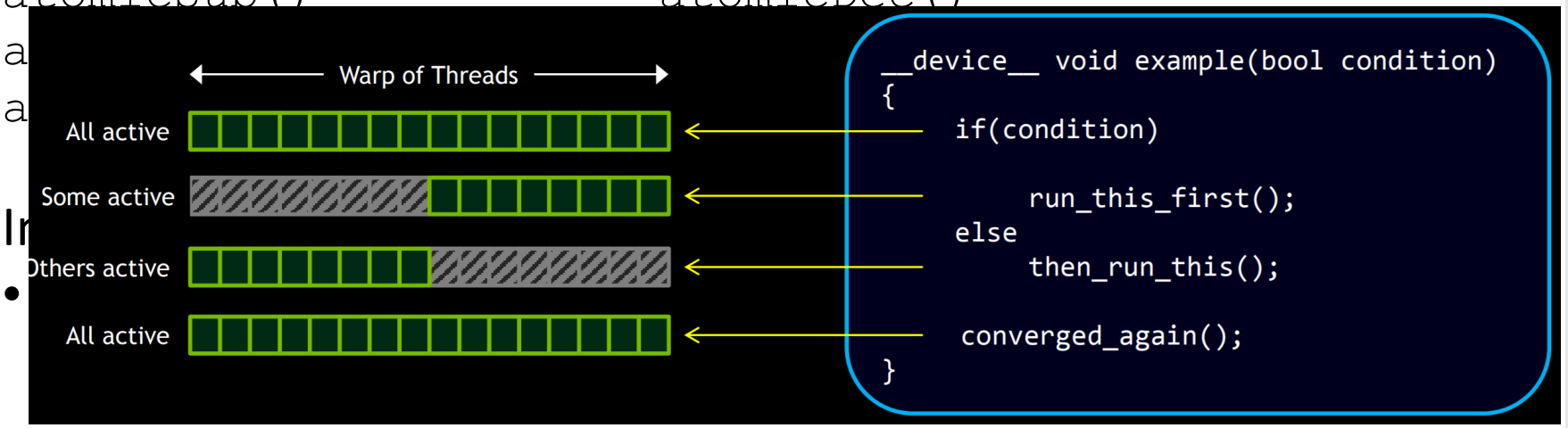

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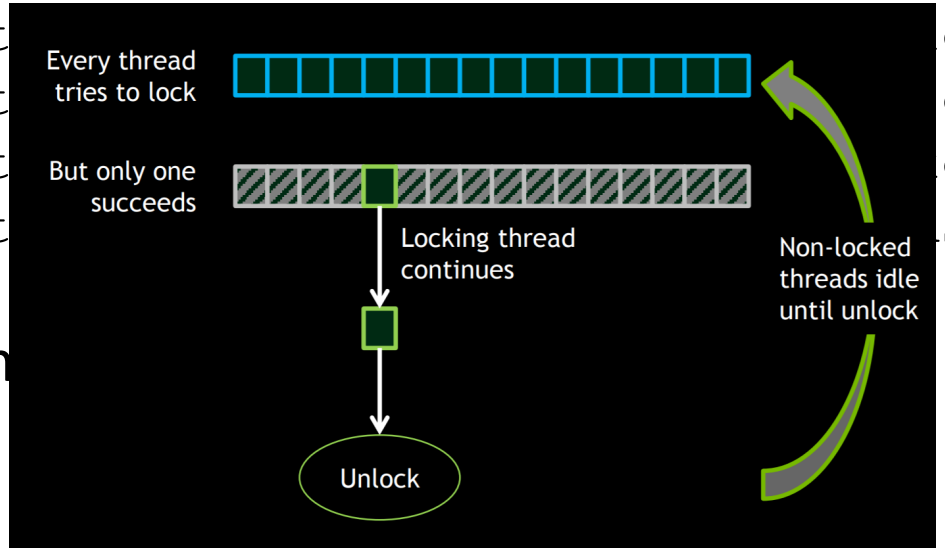

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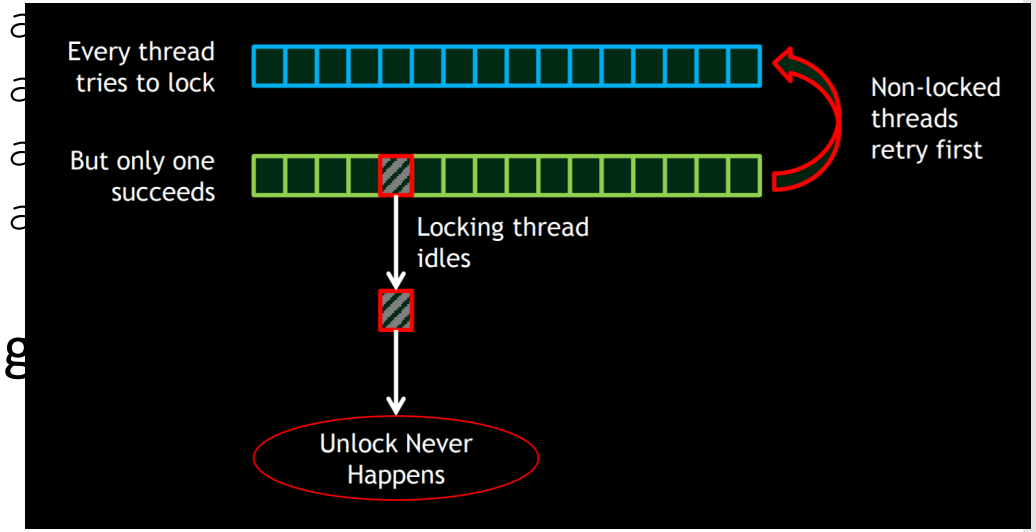
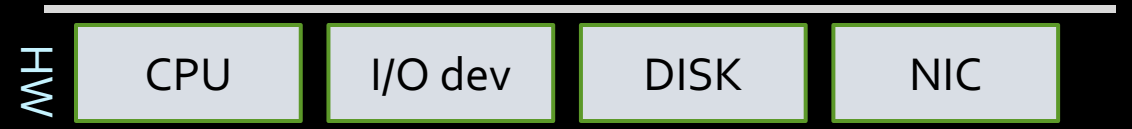


Advanced Topic: GPU Programming Models

Layered abstractions



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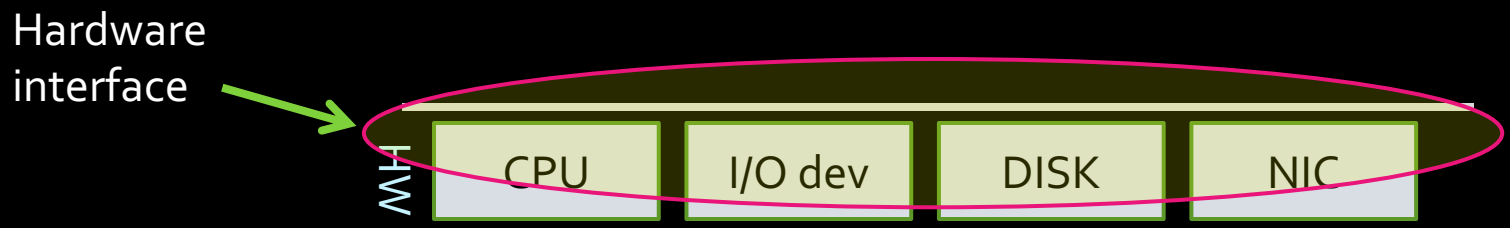

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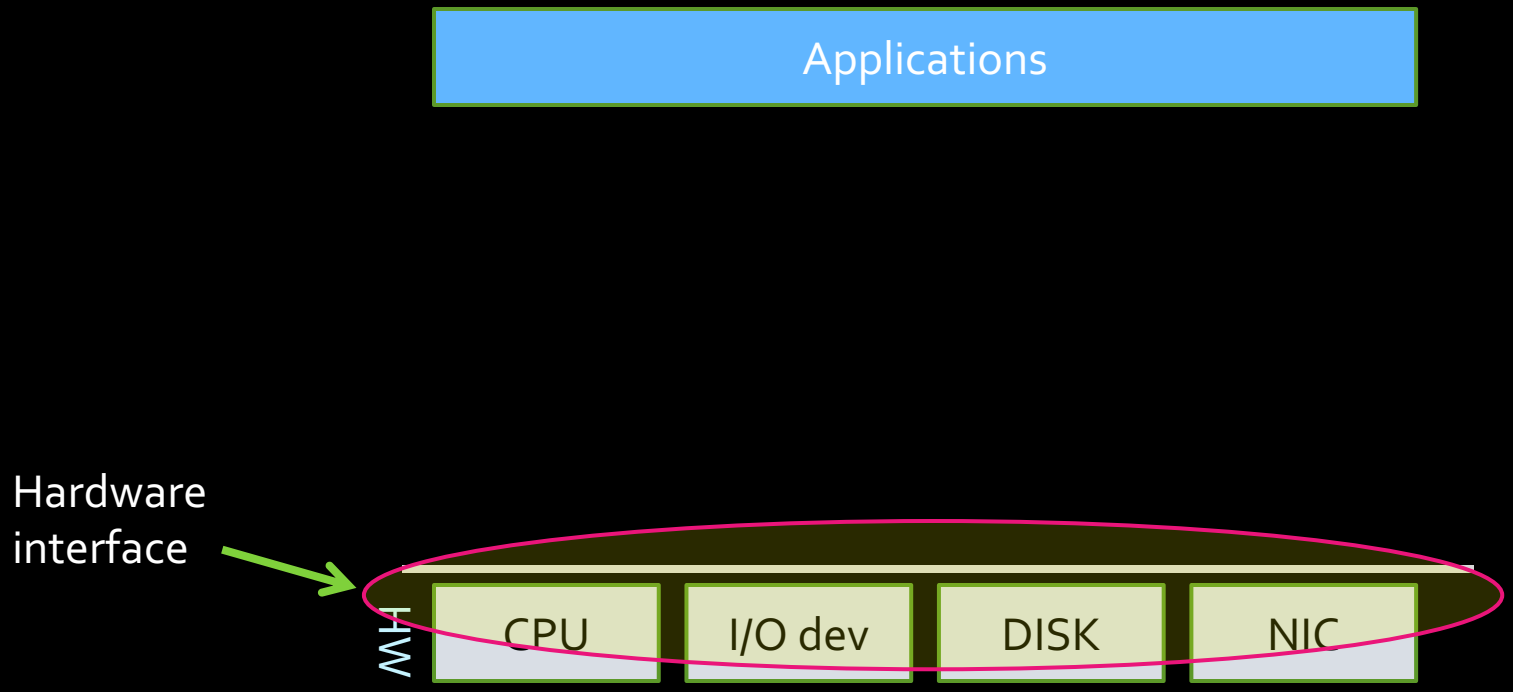

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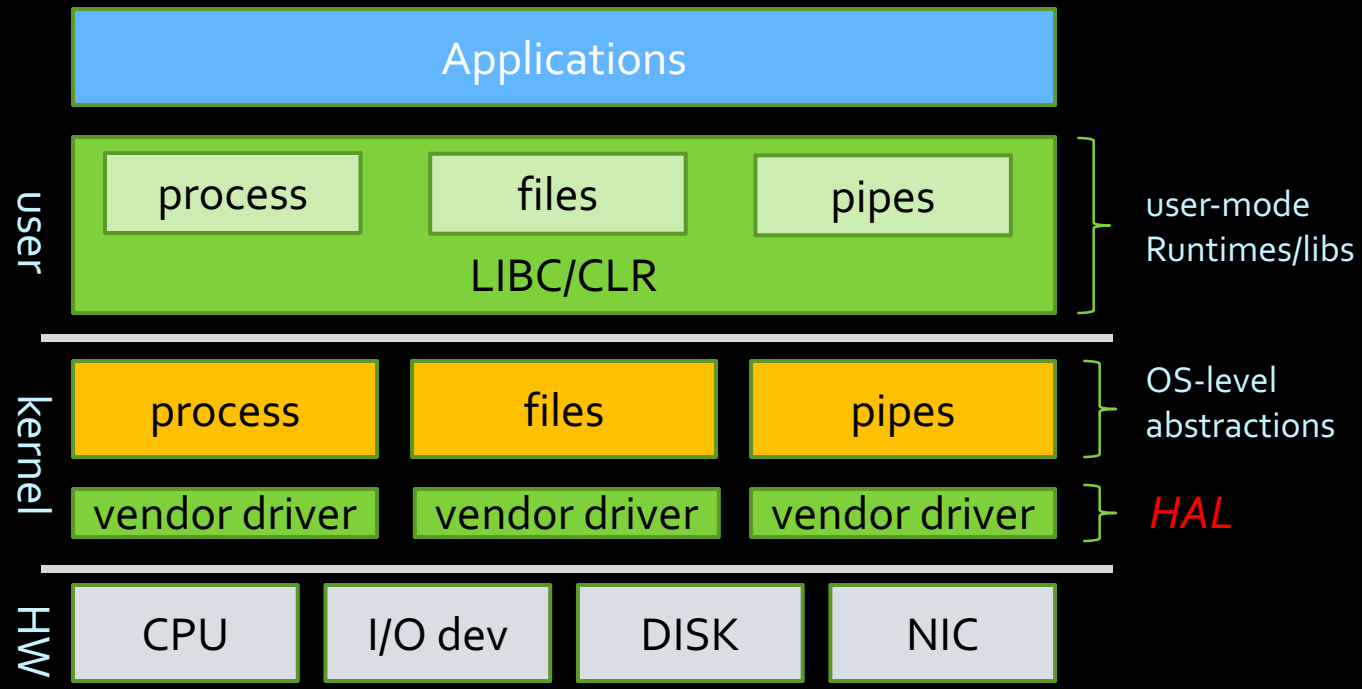

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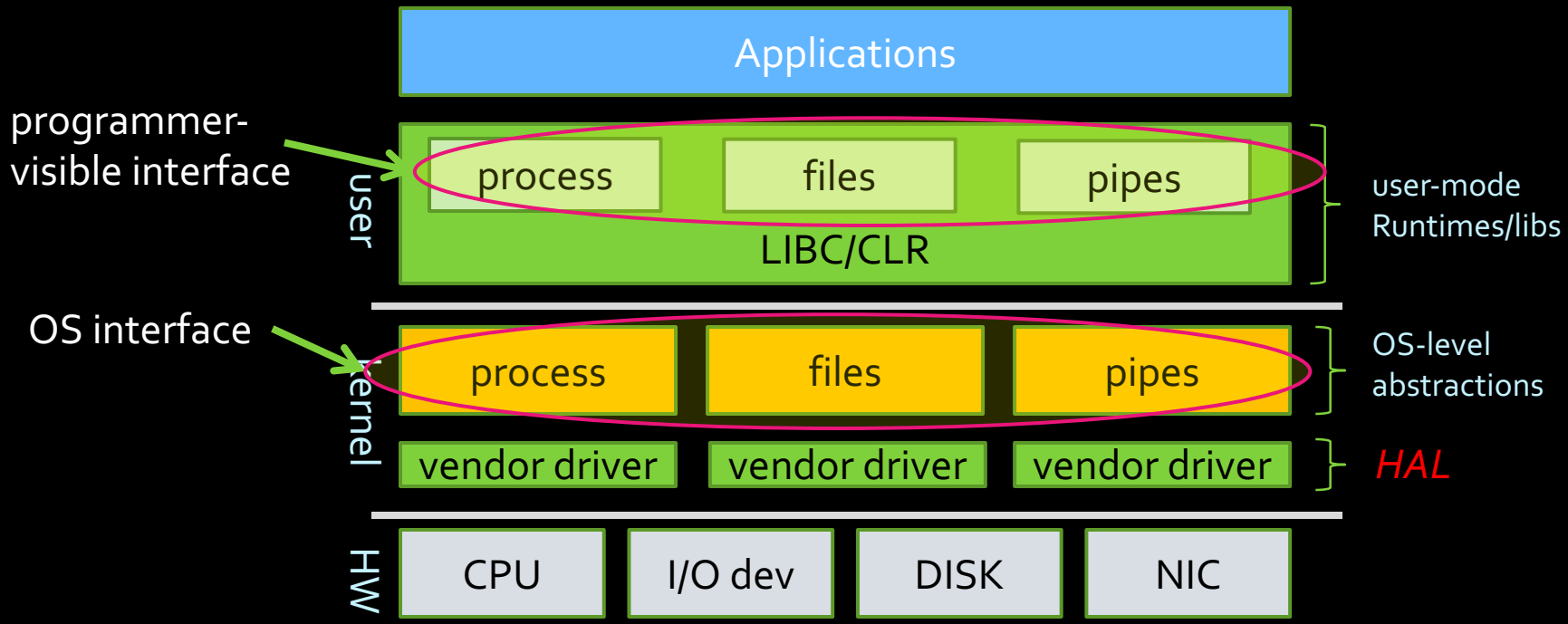

**** 1:1 correspondence between OS-level and user-level abstractions***

**** Diverse HW support enabled HAL***

GPU abstractions

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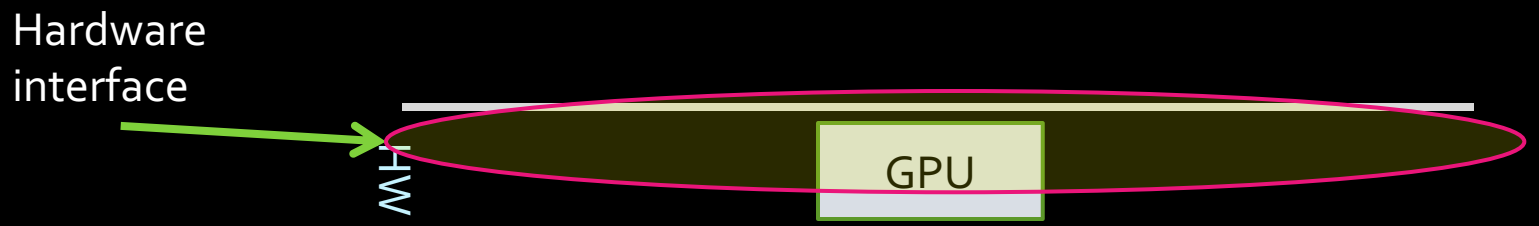

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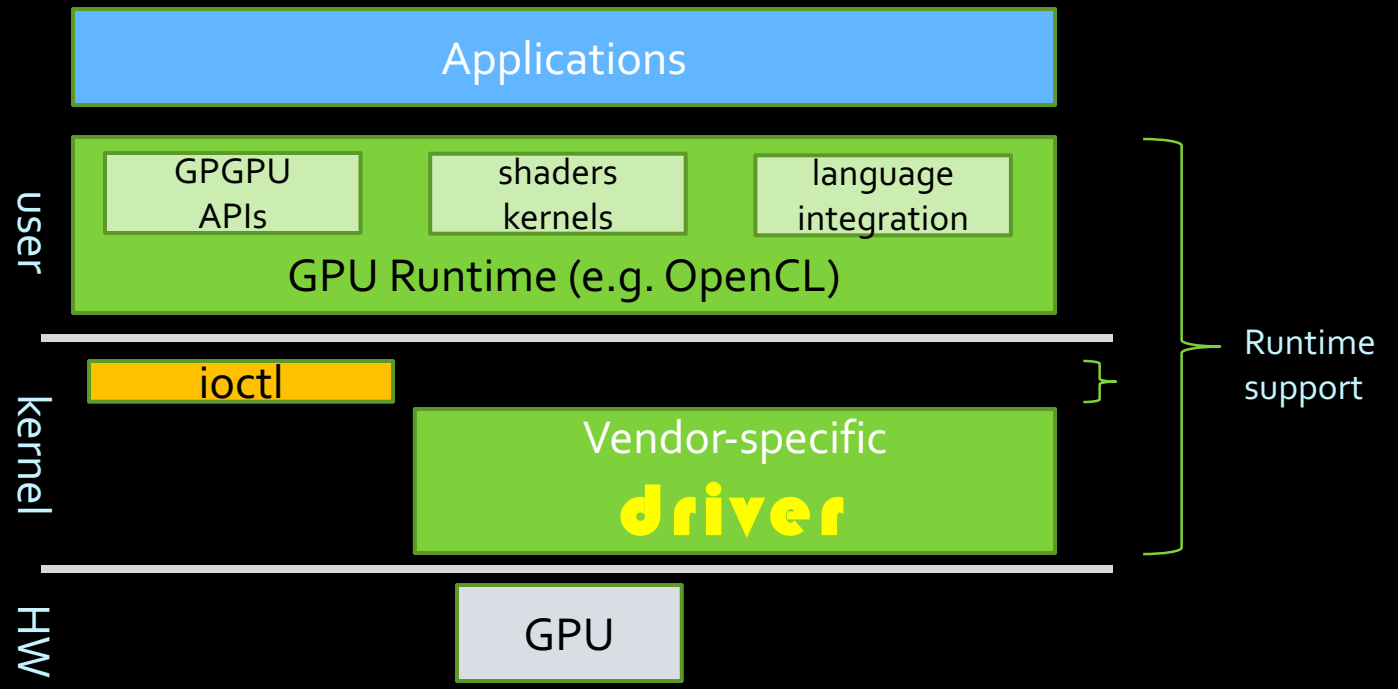

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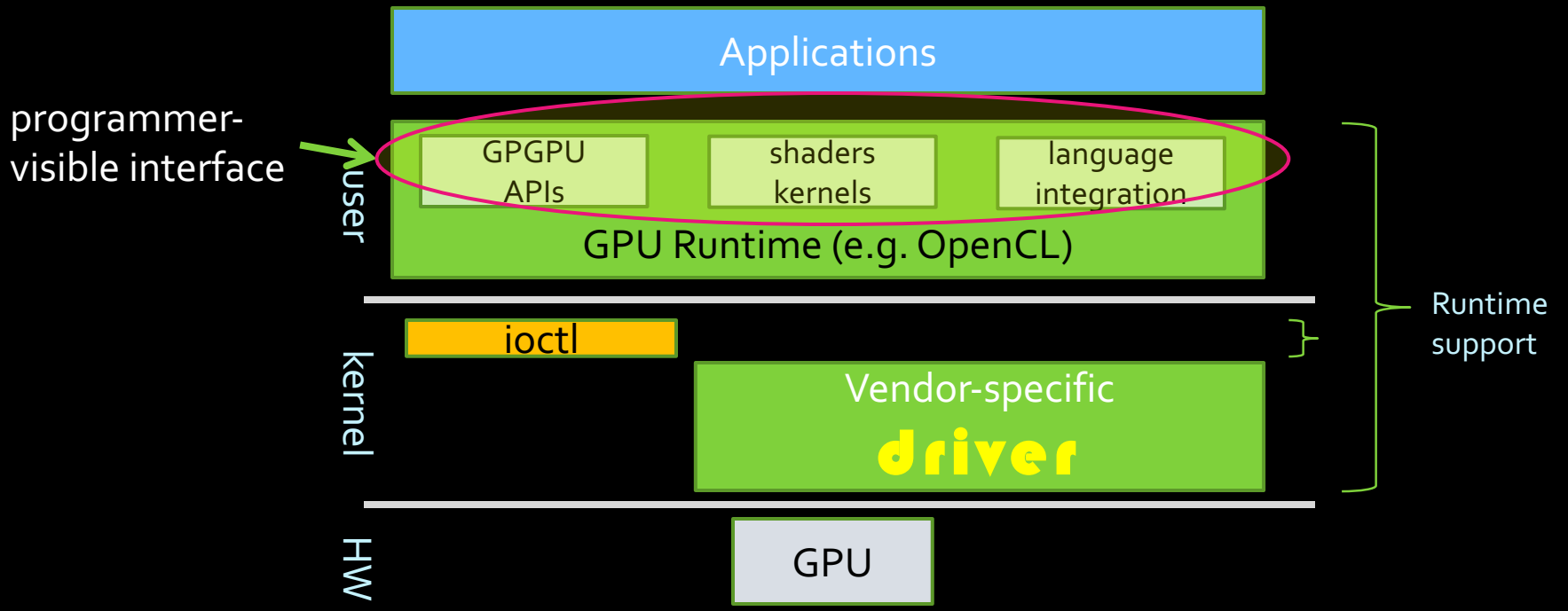

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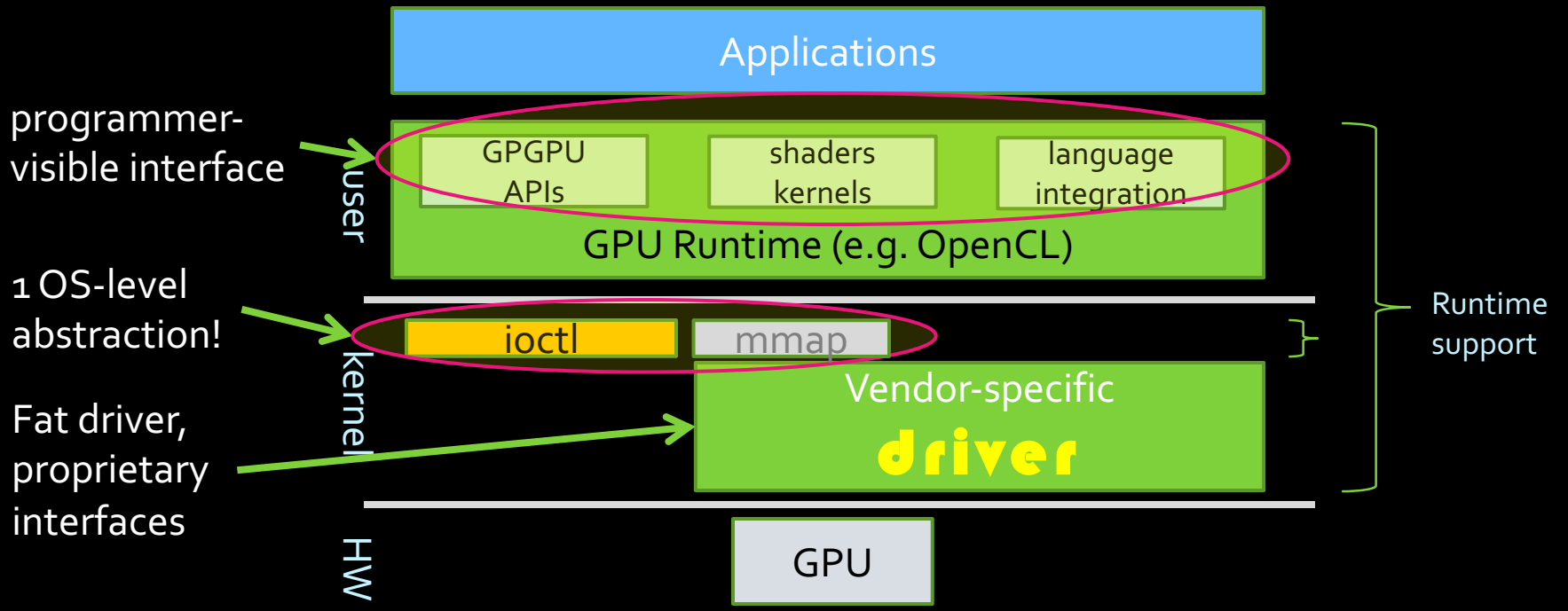

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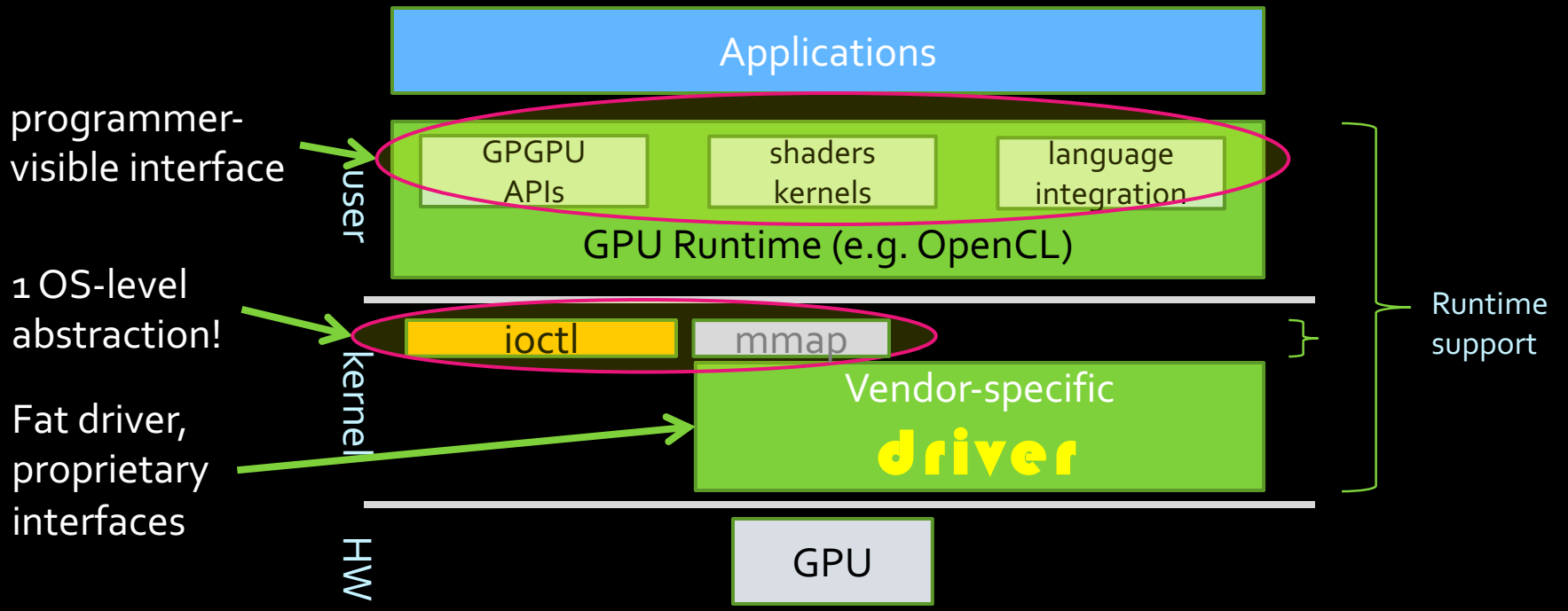
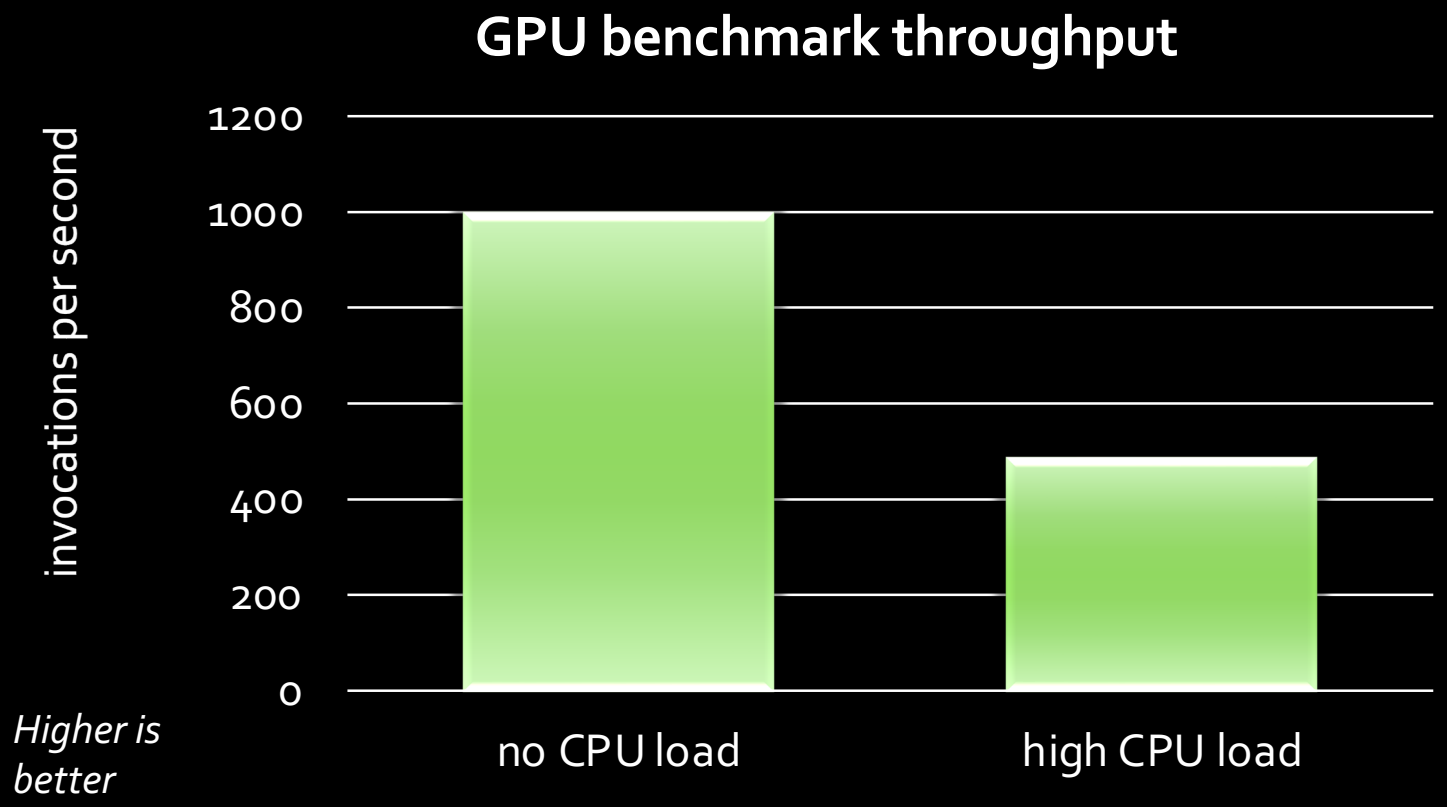


1. No kernel-facing API
2. OS resource-management limited
3. *Poor composability*

No OS support → No isolation



- Image-convolution in CUDA
- Windows 7 x64 8GB RAM
- Intel Core 2 Quad 2.66GHz
- nVidia GeForce GT230

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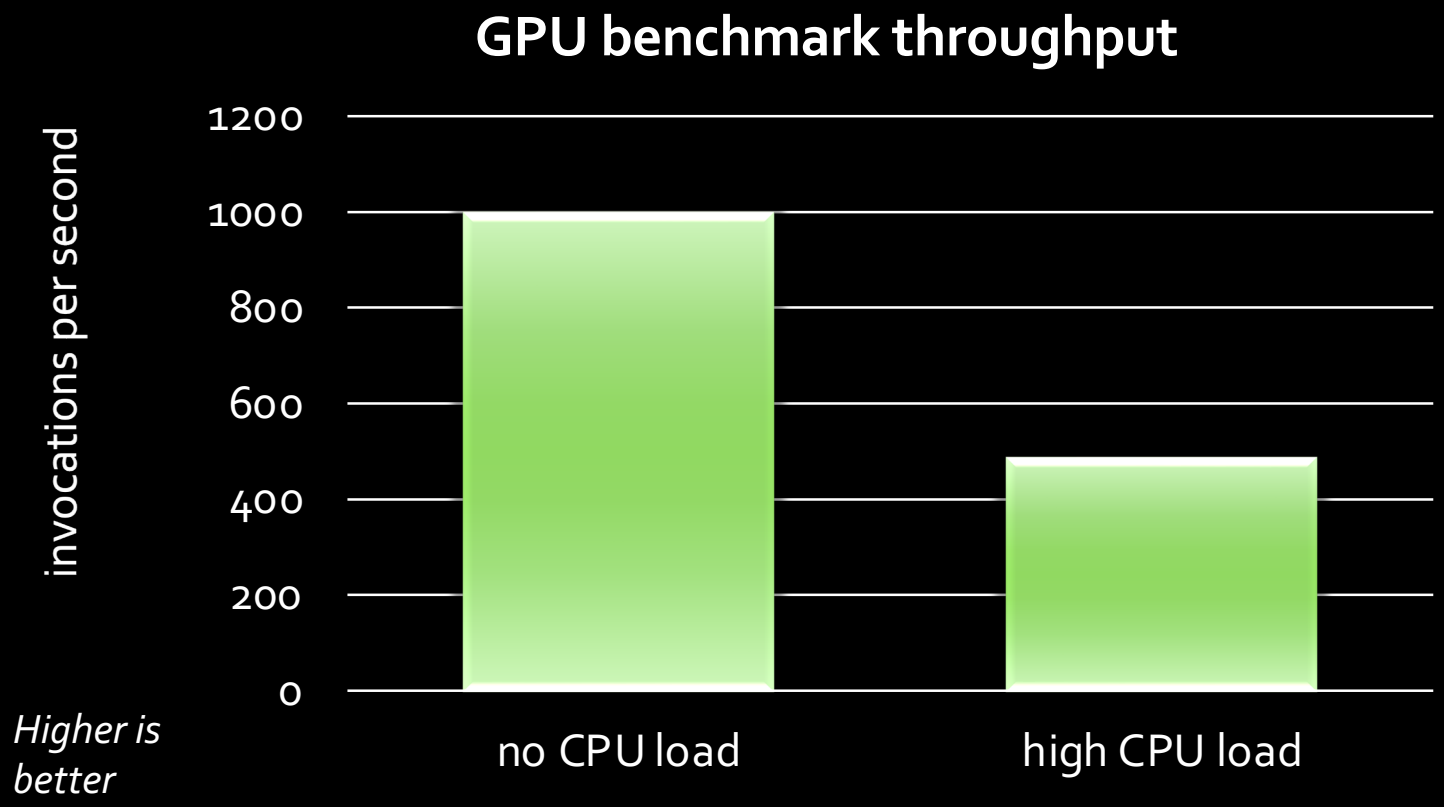

CPU+GPU schedulers not integrated!
…other pathologies abundant

ge-convolution in CUDA
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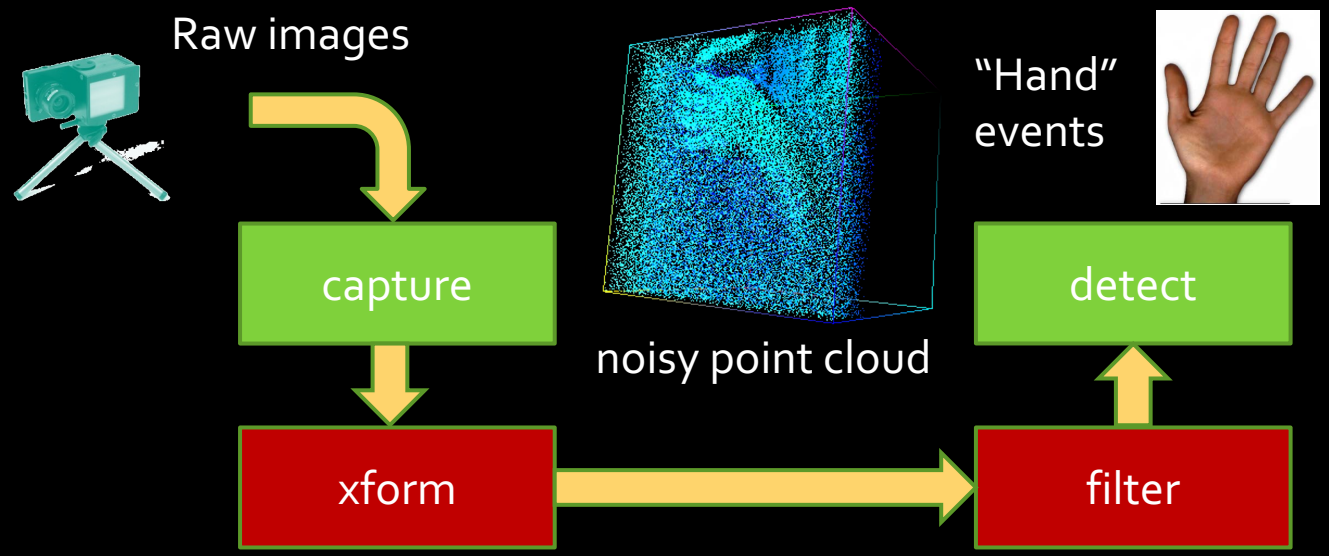
Composition: Gestural Interface



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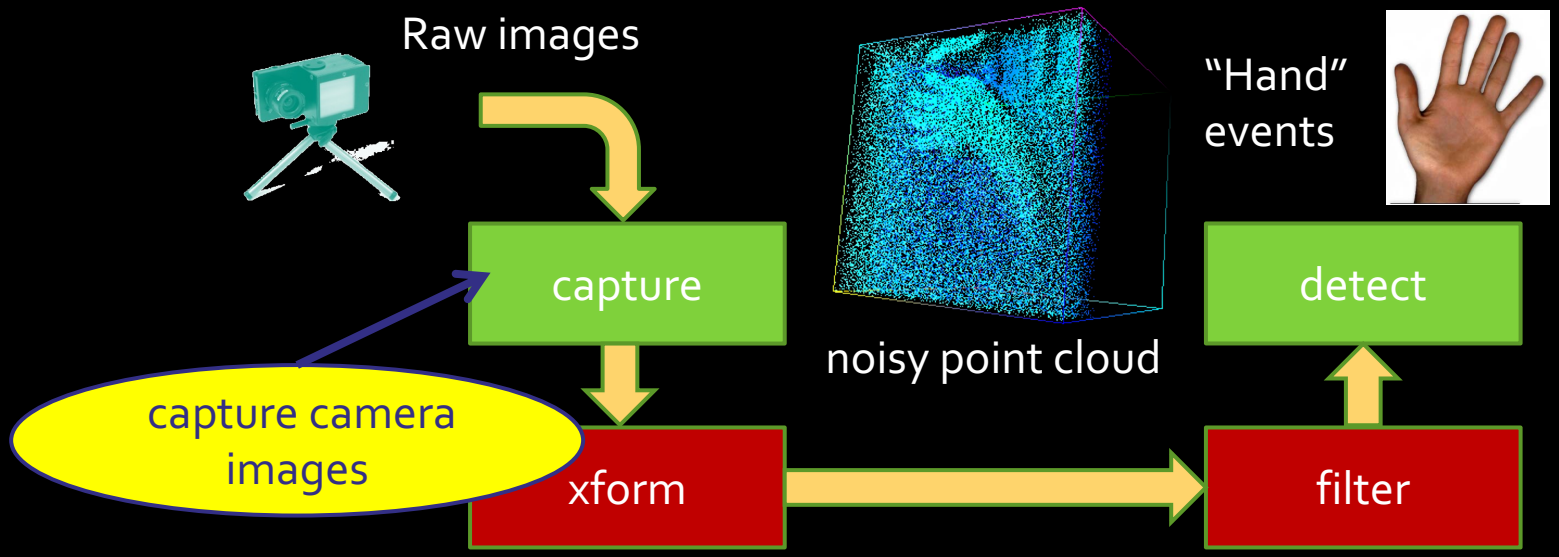

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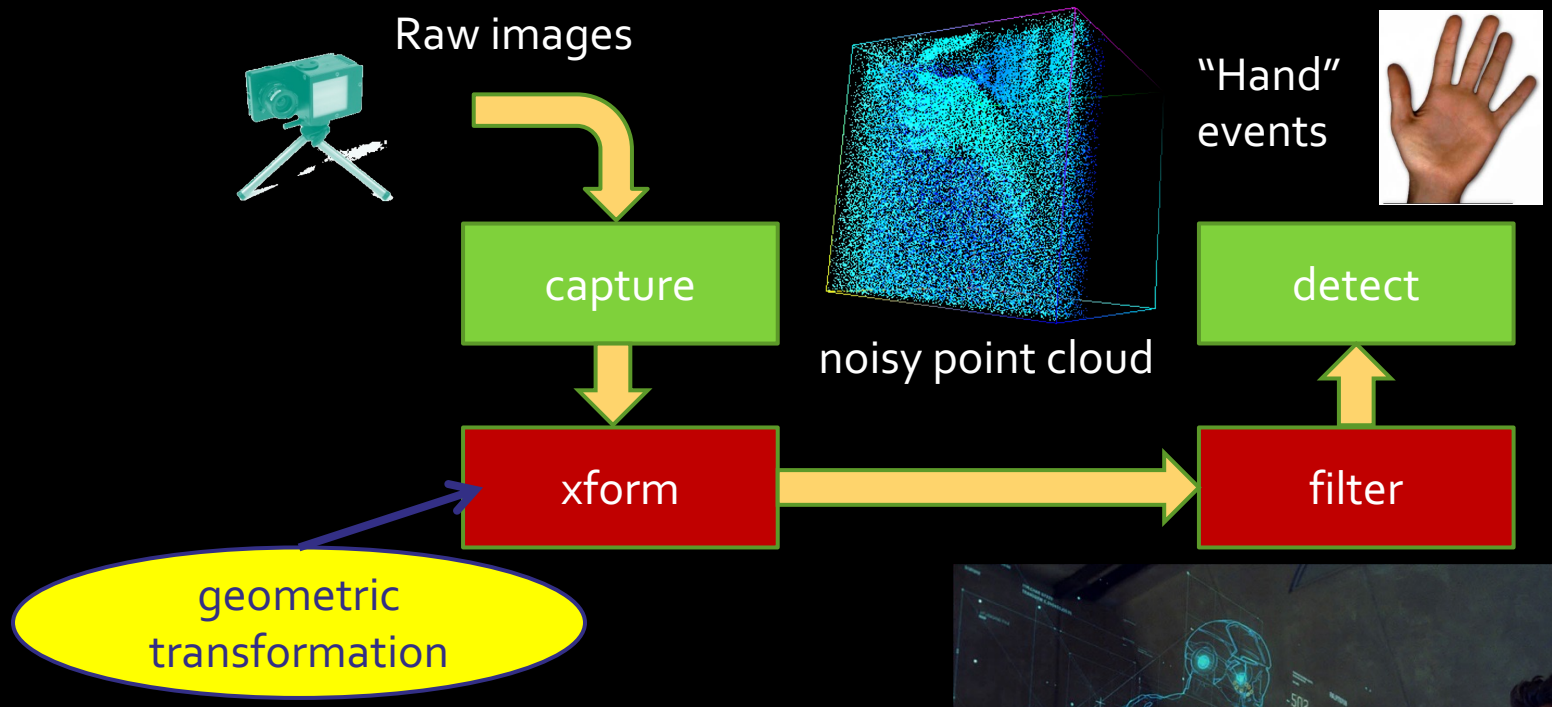
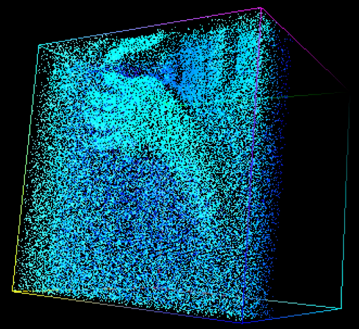


Composition: Gestural Interface

Raw images

capture

xform

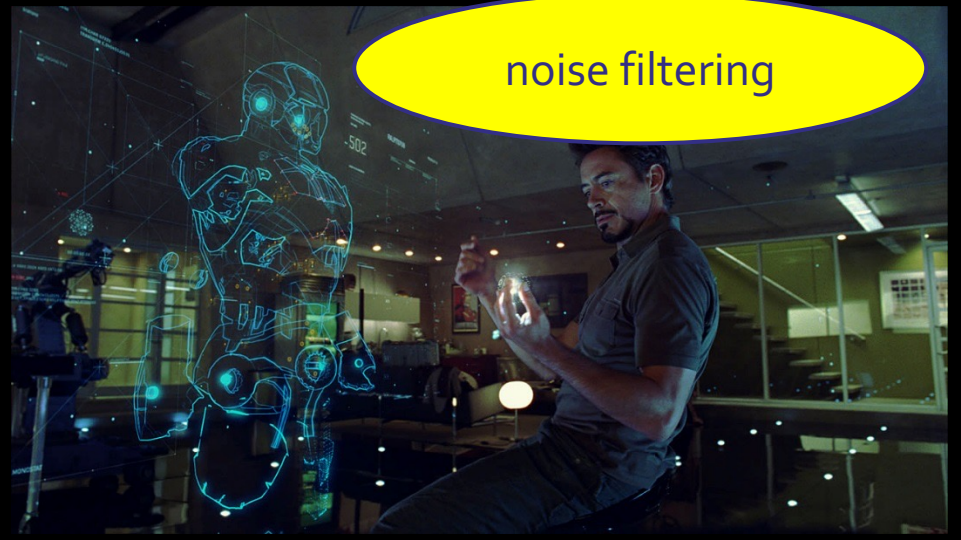


noisy point cloud

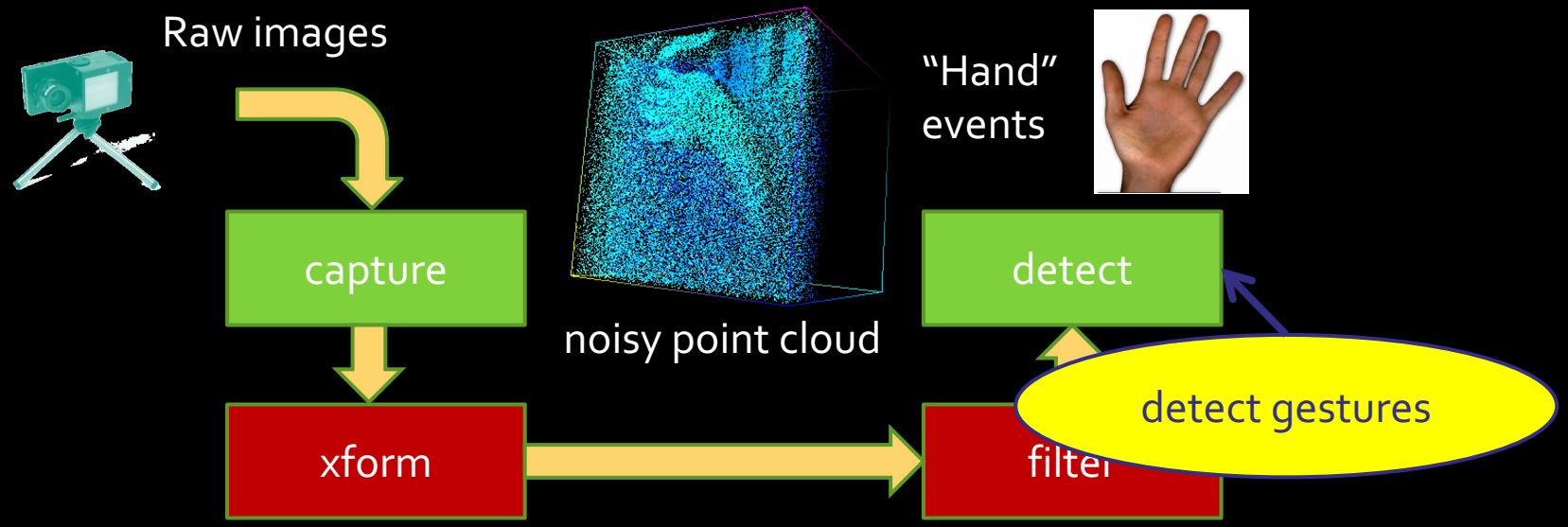
filter

detect

"Hand" events



Composition: Gestural Interface



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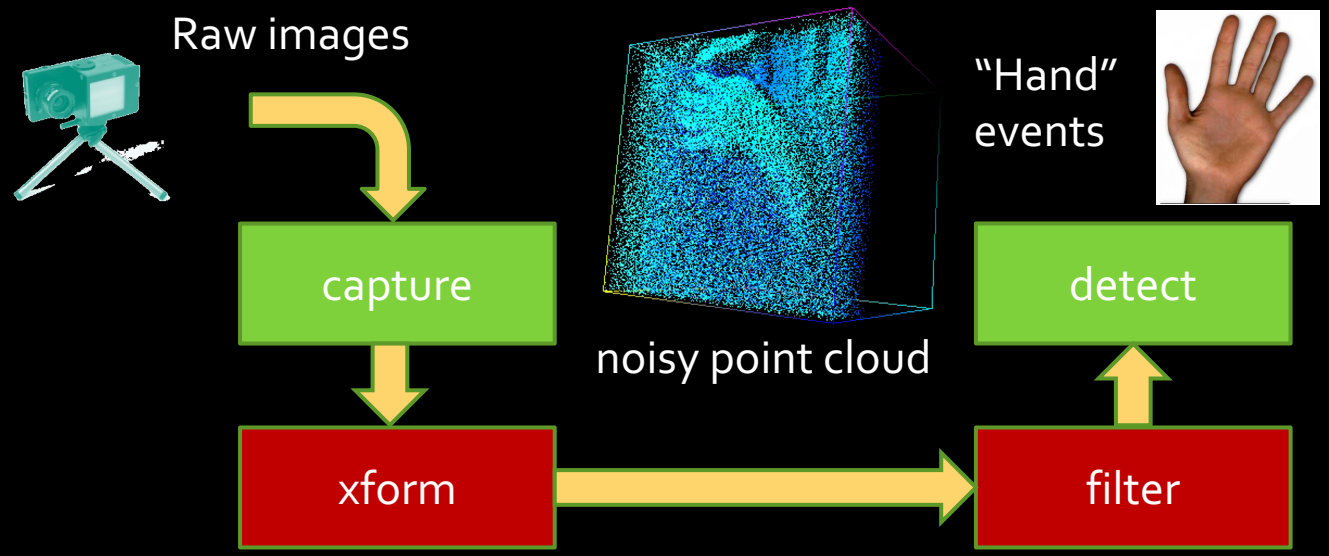

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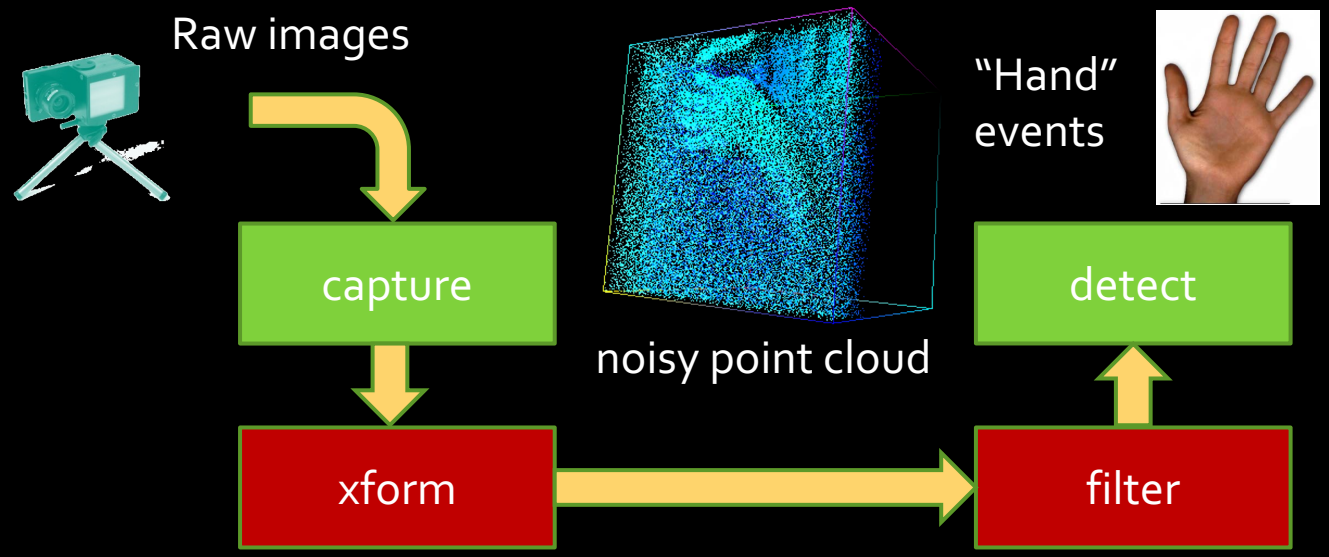

- Requires OS mediation
- High data rates
- Abundant data parallelism

  …use GPUs!

What We'd Like To Do

```
#> capture | xform | filter | detect &
```

- Modular design
  - flexibility, reuse
- Utilize heterogeneous hardware
  - Data-parallel components → GPU
  - Sequential components → CPU
- Using OS provided tools
  - processes, pipes

What We'd Like To Do

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CPU GPU GPU CPU

- Modular design
  - flexibility, reuse
- Utilize heterogeneous hardware
  - Data-parallel components → GPU
  - Sequential components → CPU
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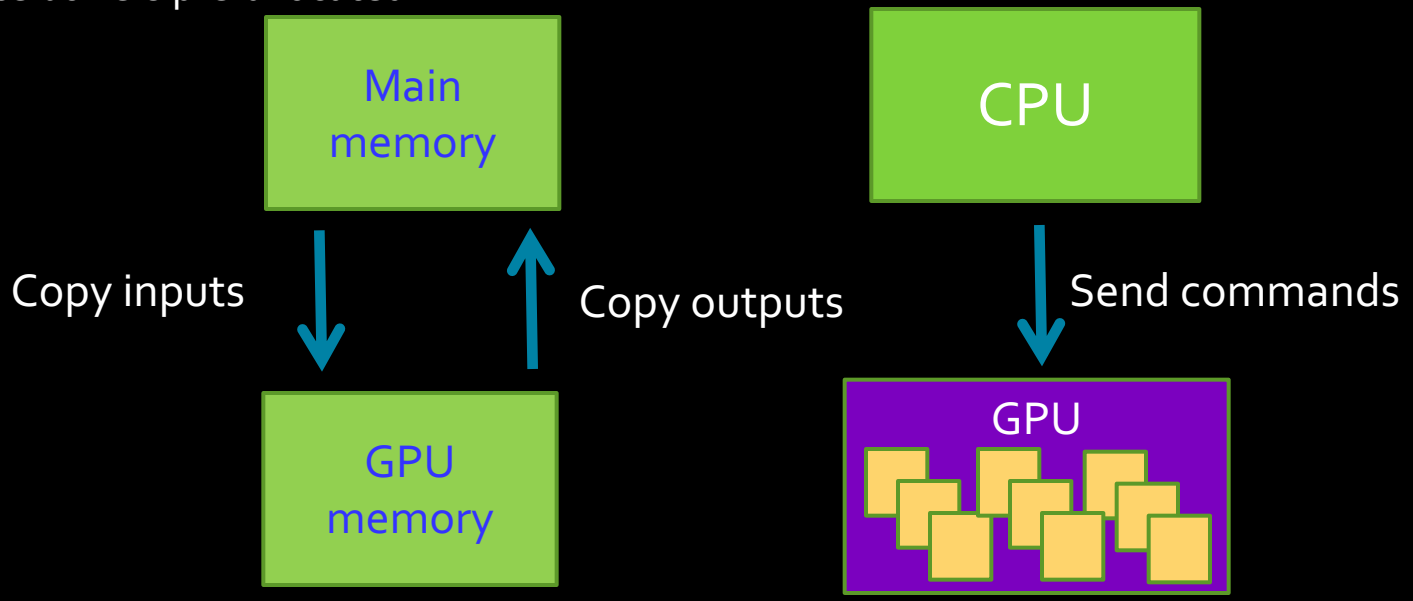
GPU Execution model

- GPUs cannot run OS:
  - different ISA
  - Memories have different coherence guarantees
    - **(disjoint, or require fence instructions)**
- Host CPU must "manage" GPU execution
  - Program inputs explicitly transferred/bound at runtime
  - Device buffers pre-allocated



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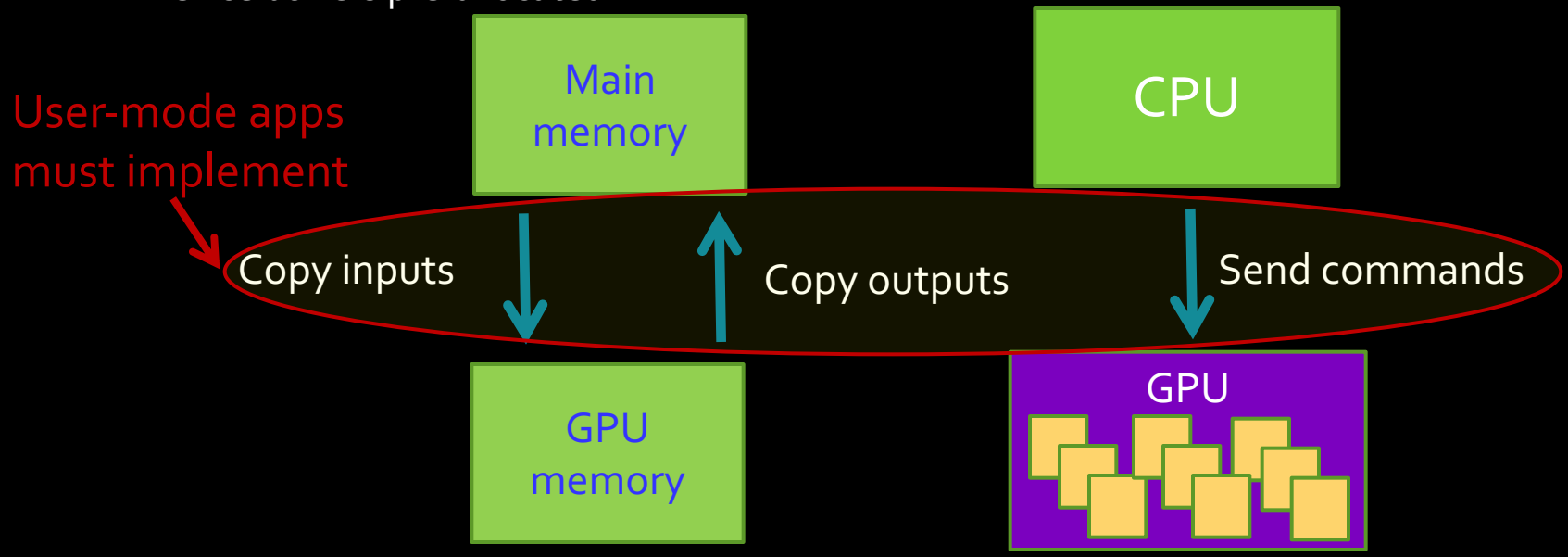

Data migration

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#> capture | xform | filter | detect &
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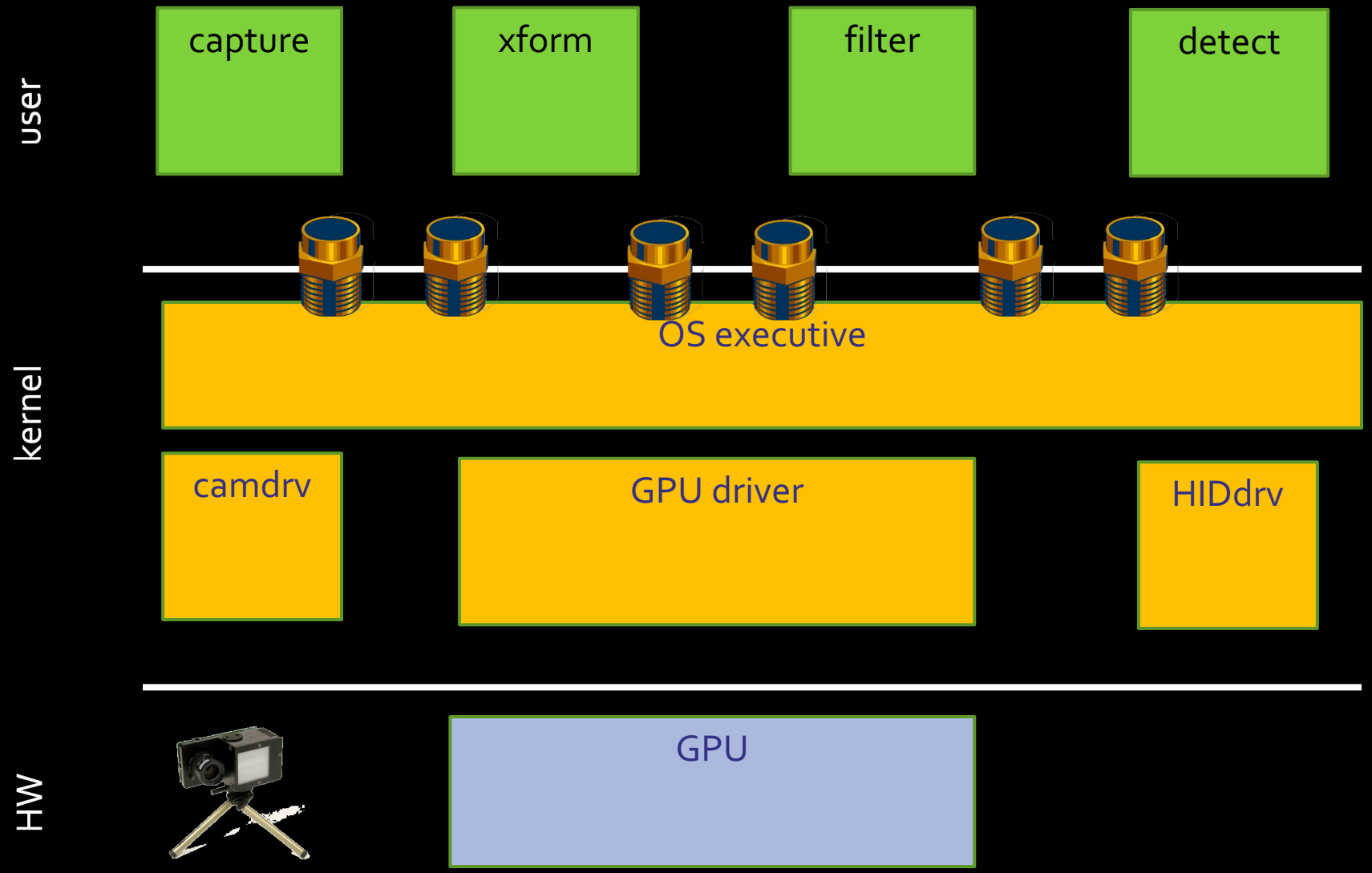

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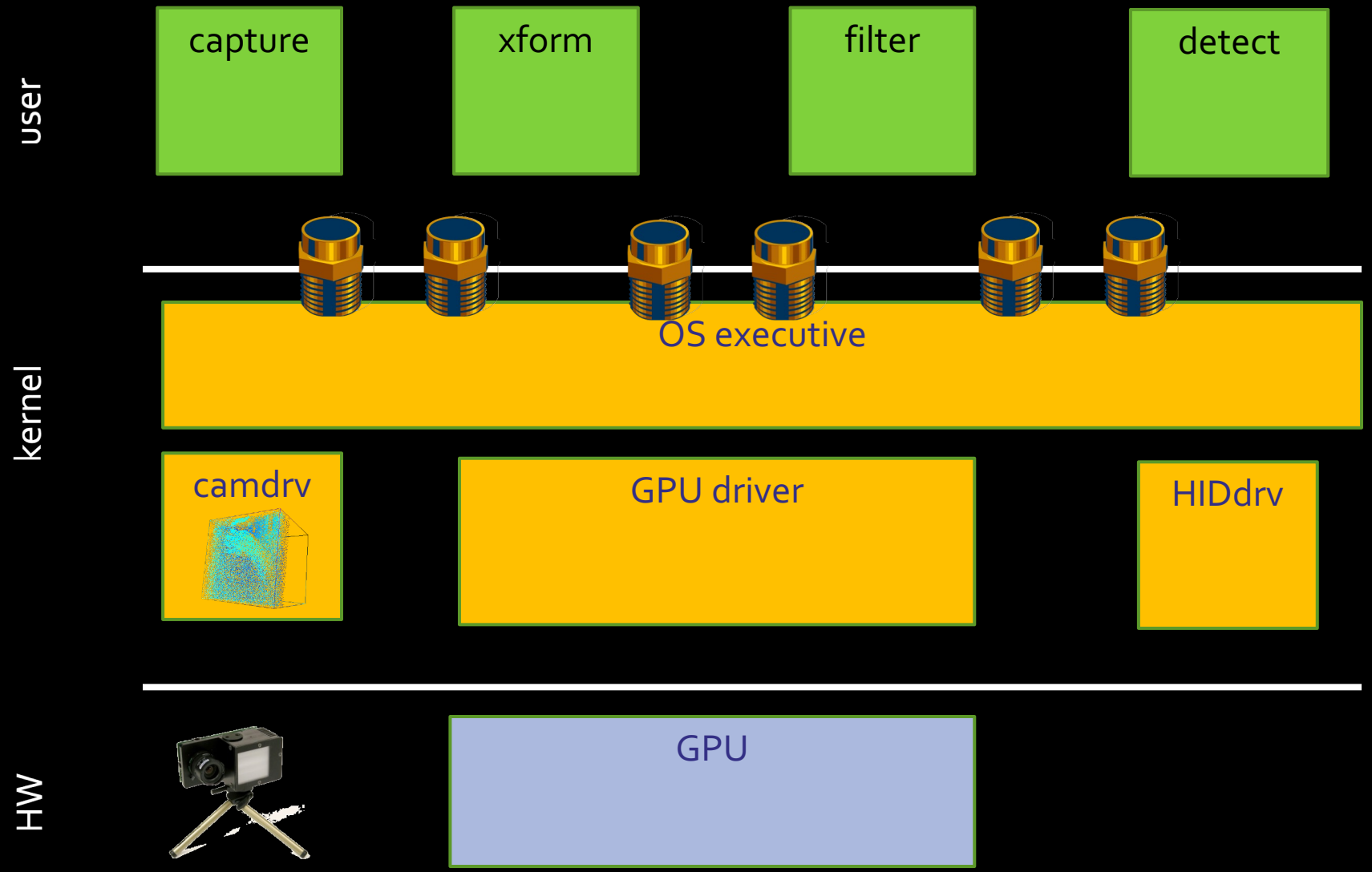

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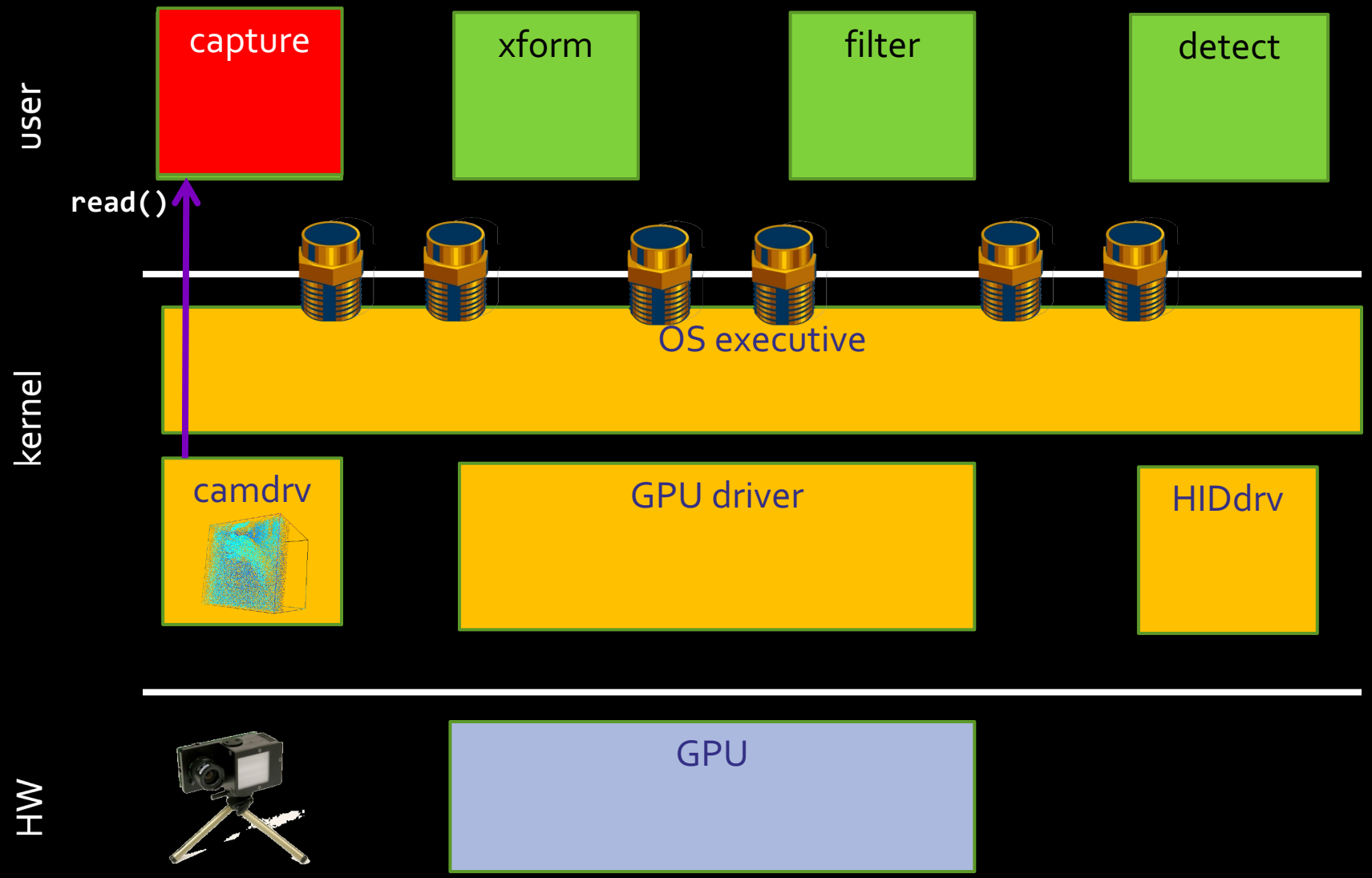

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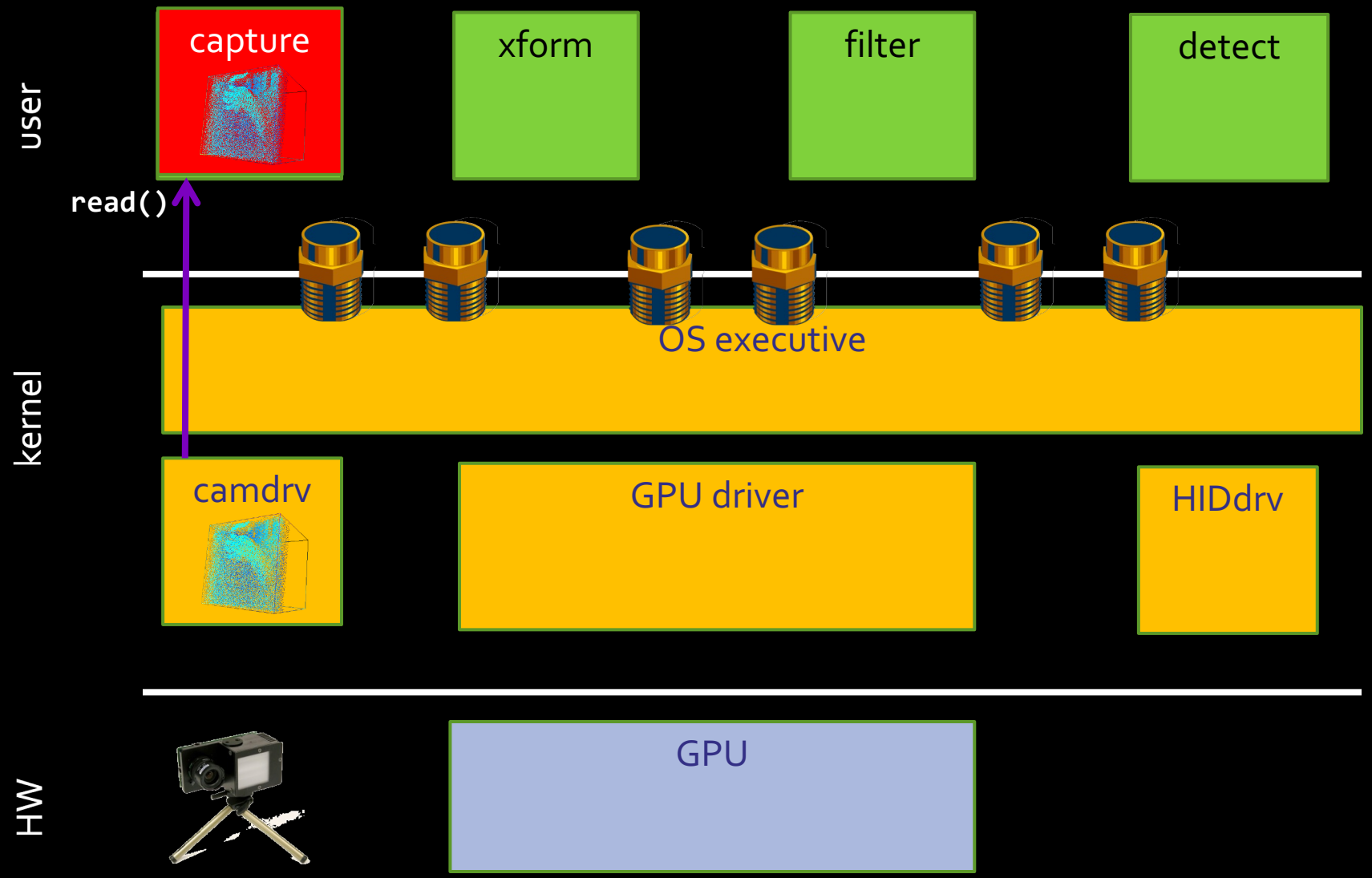

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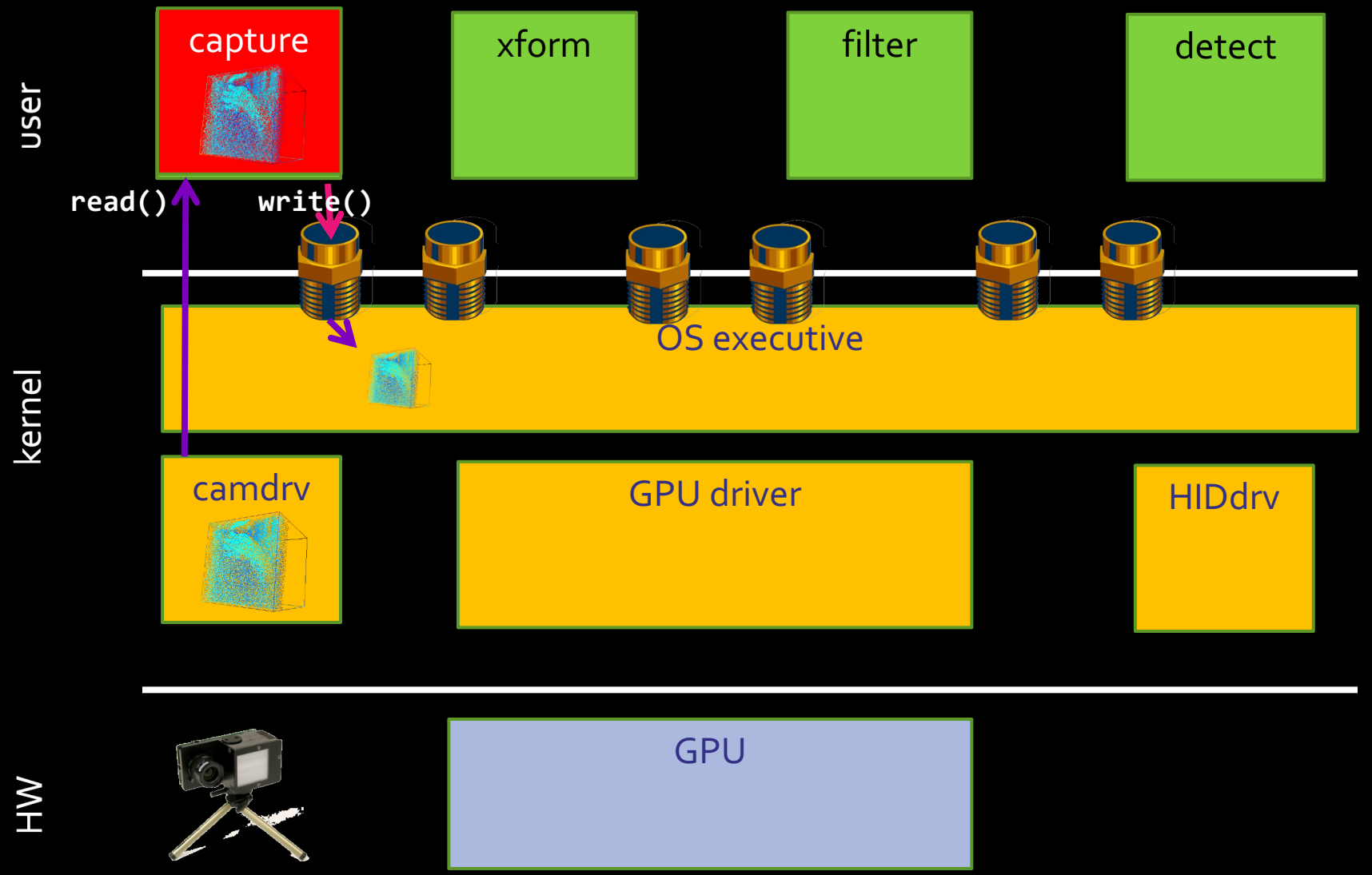

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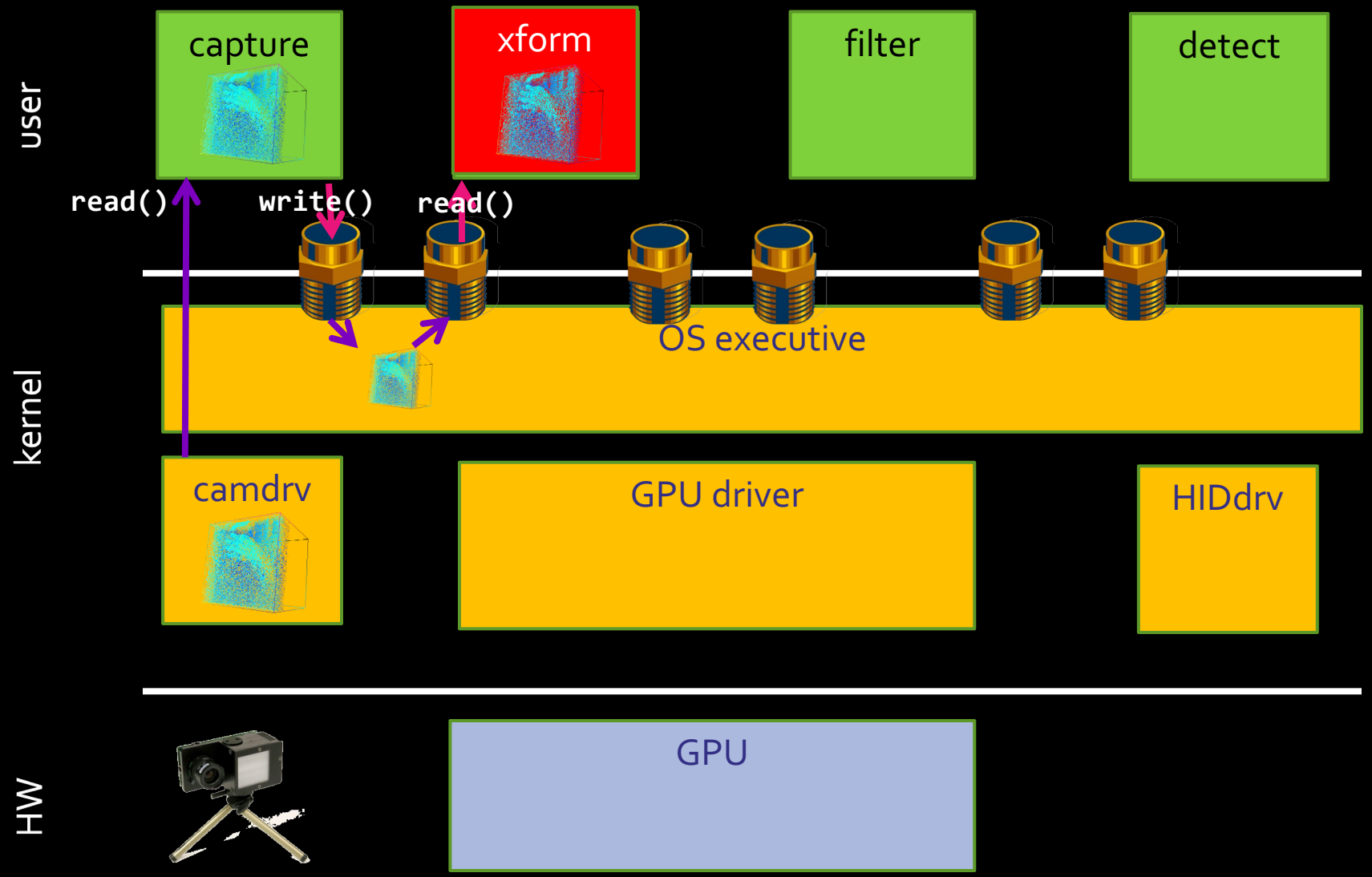

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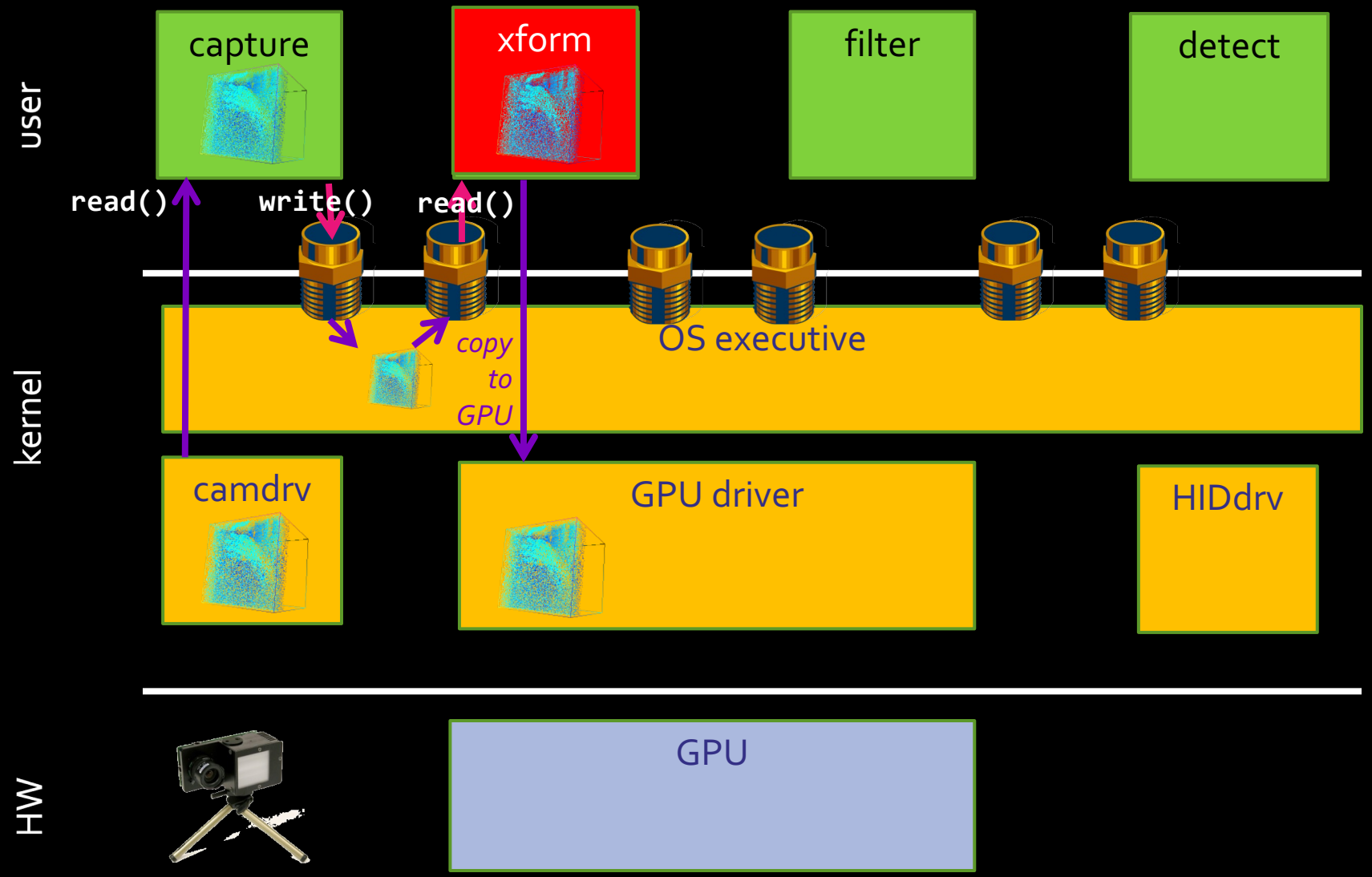

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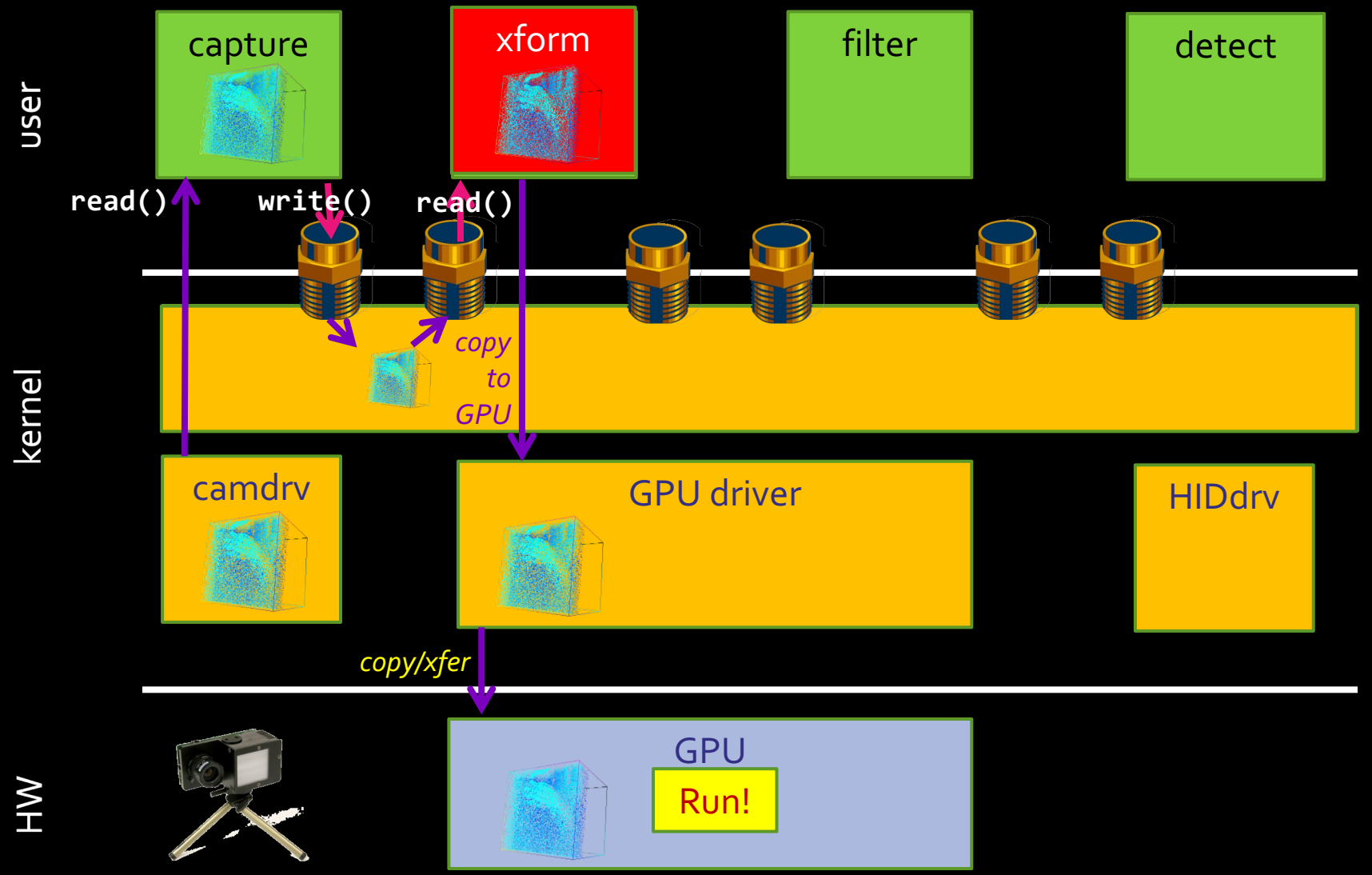

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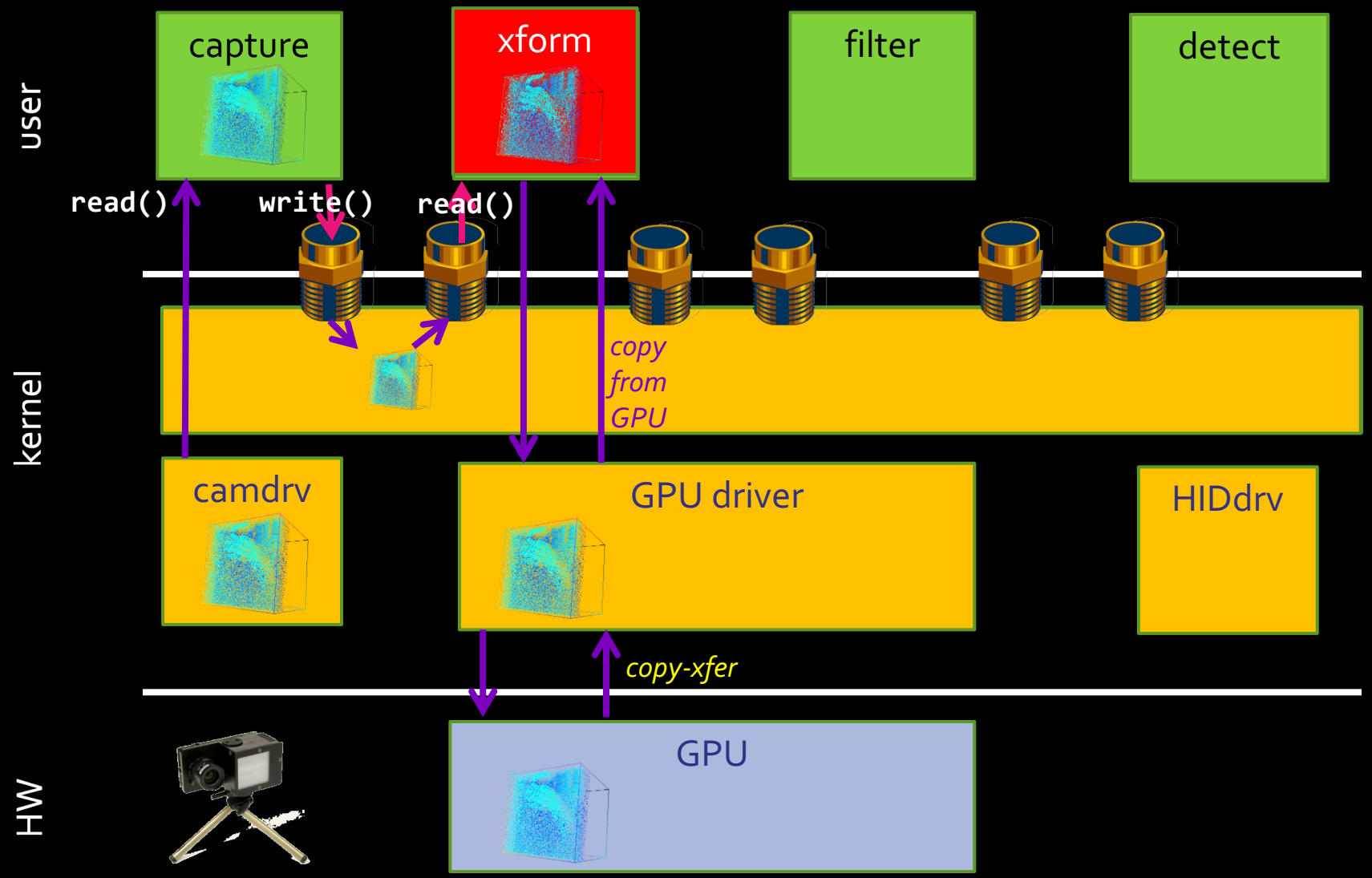

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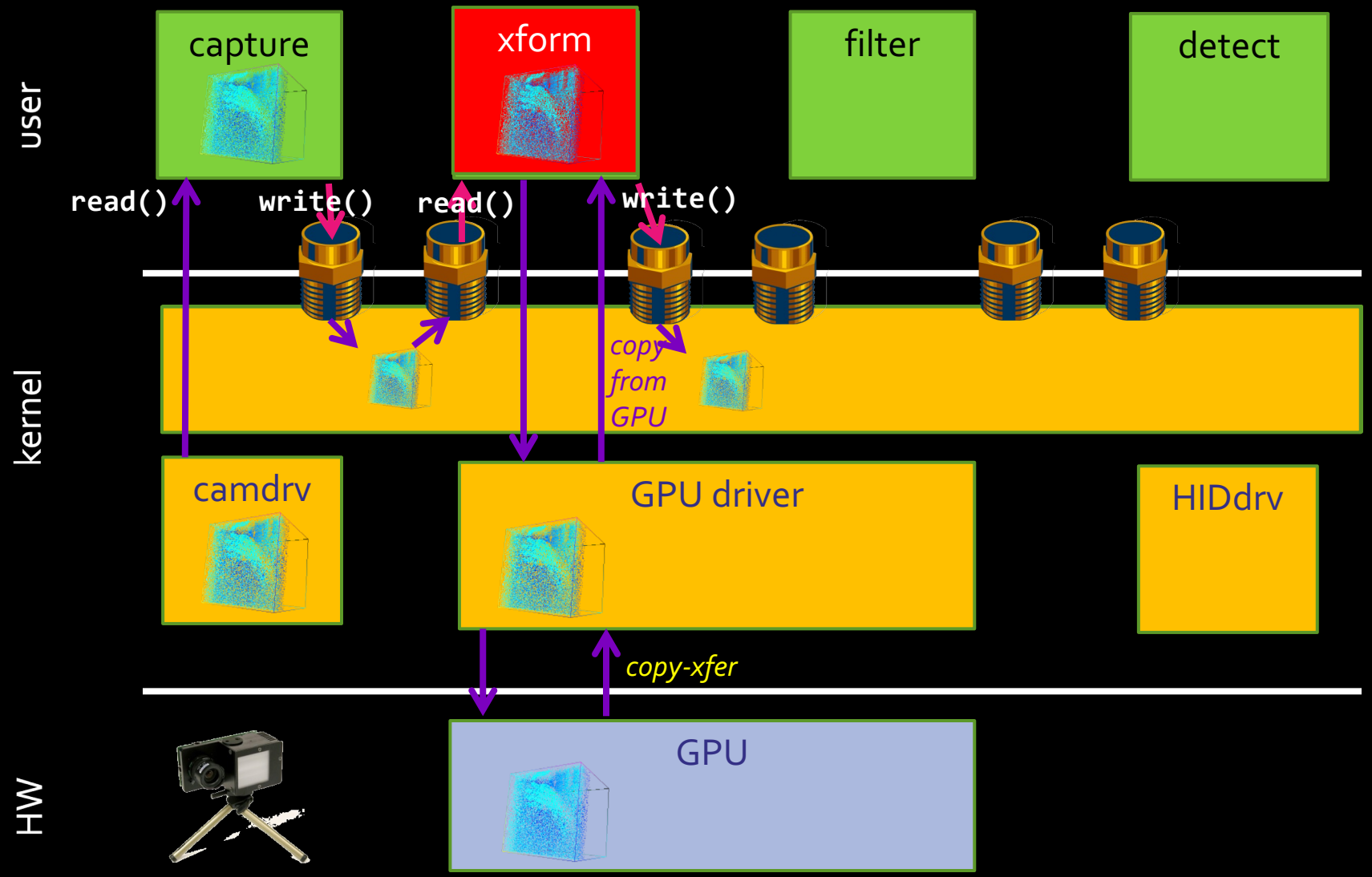

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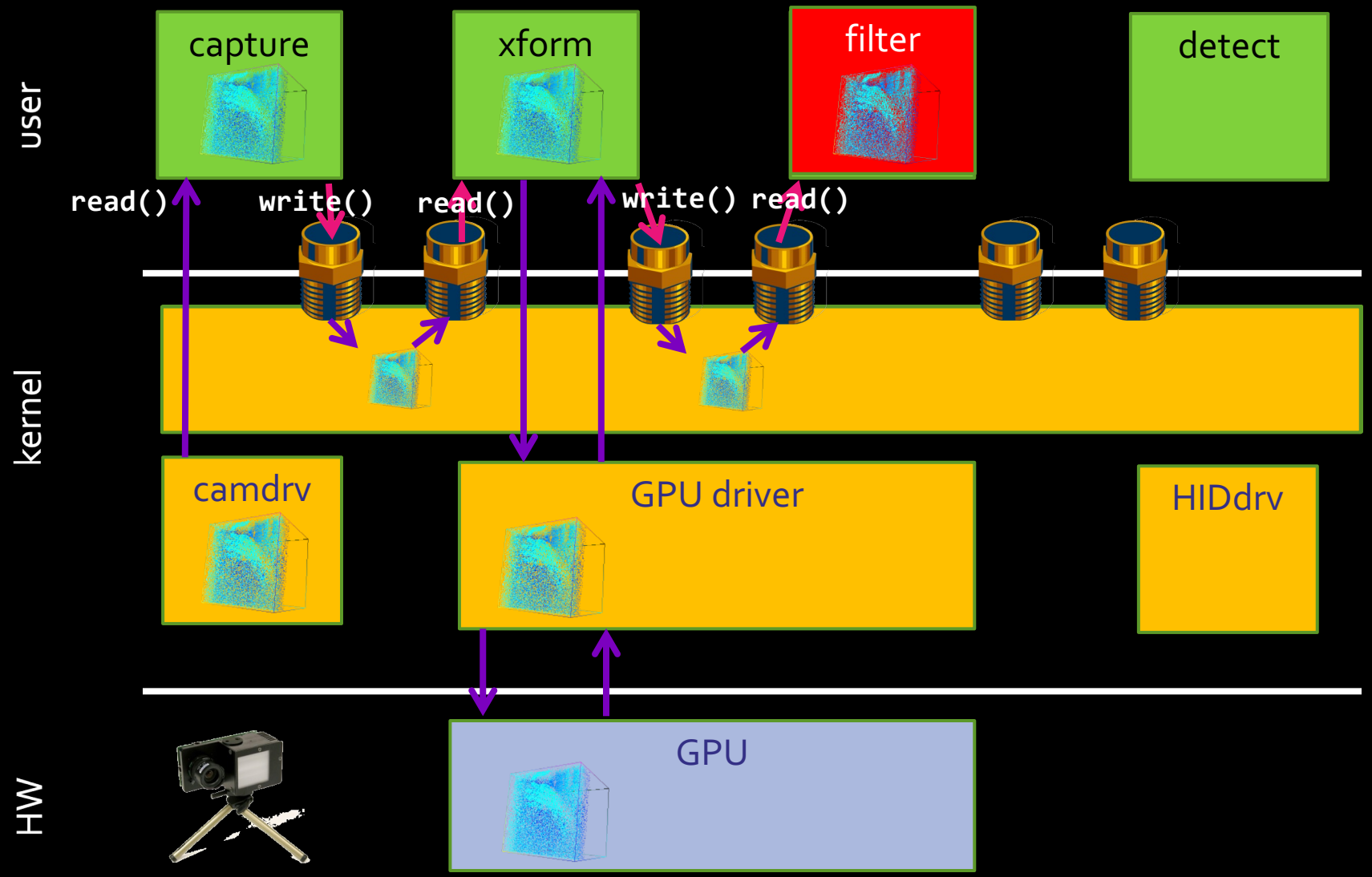

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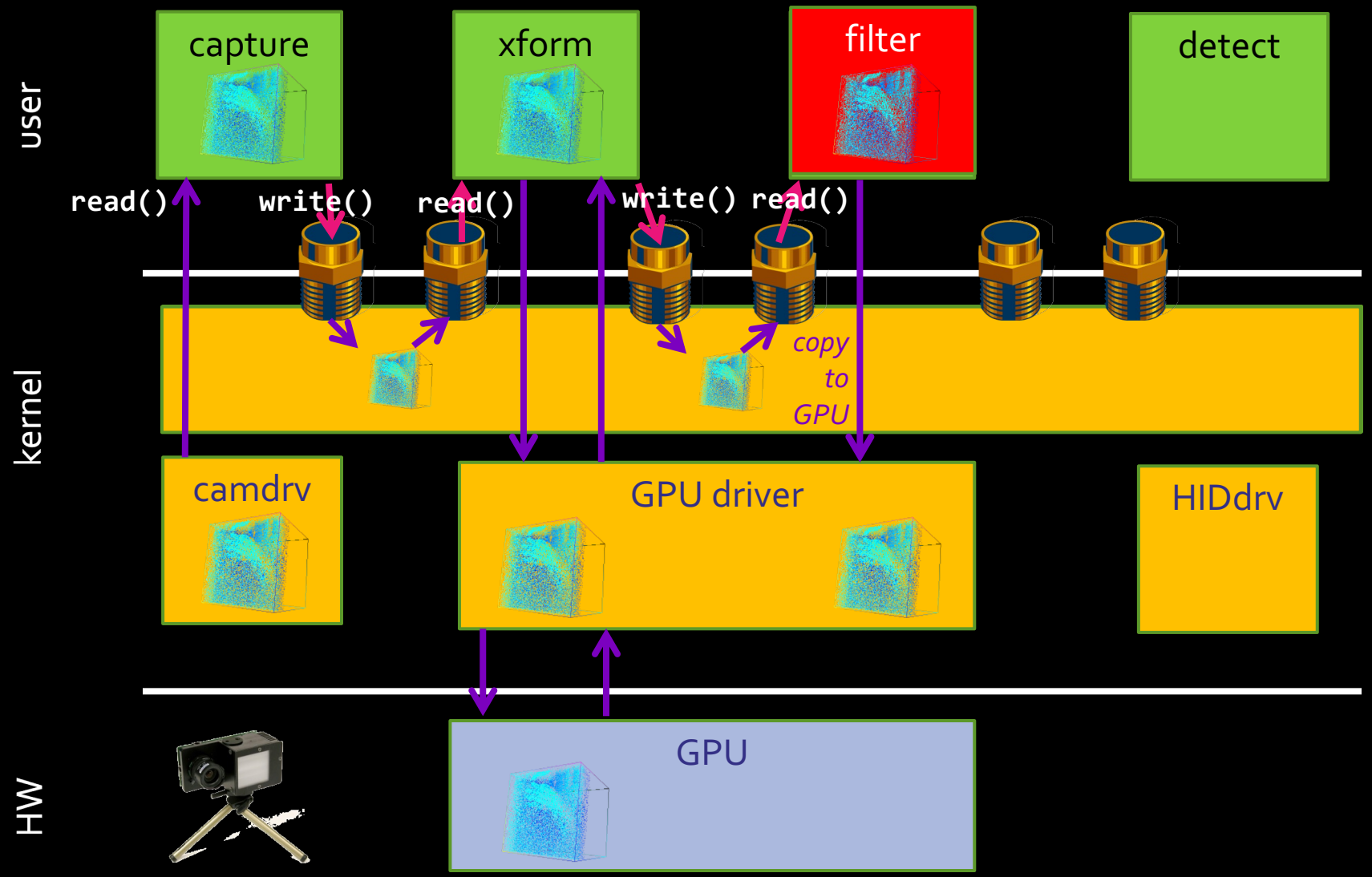

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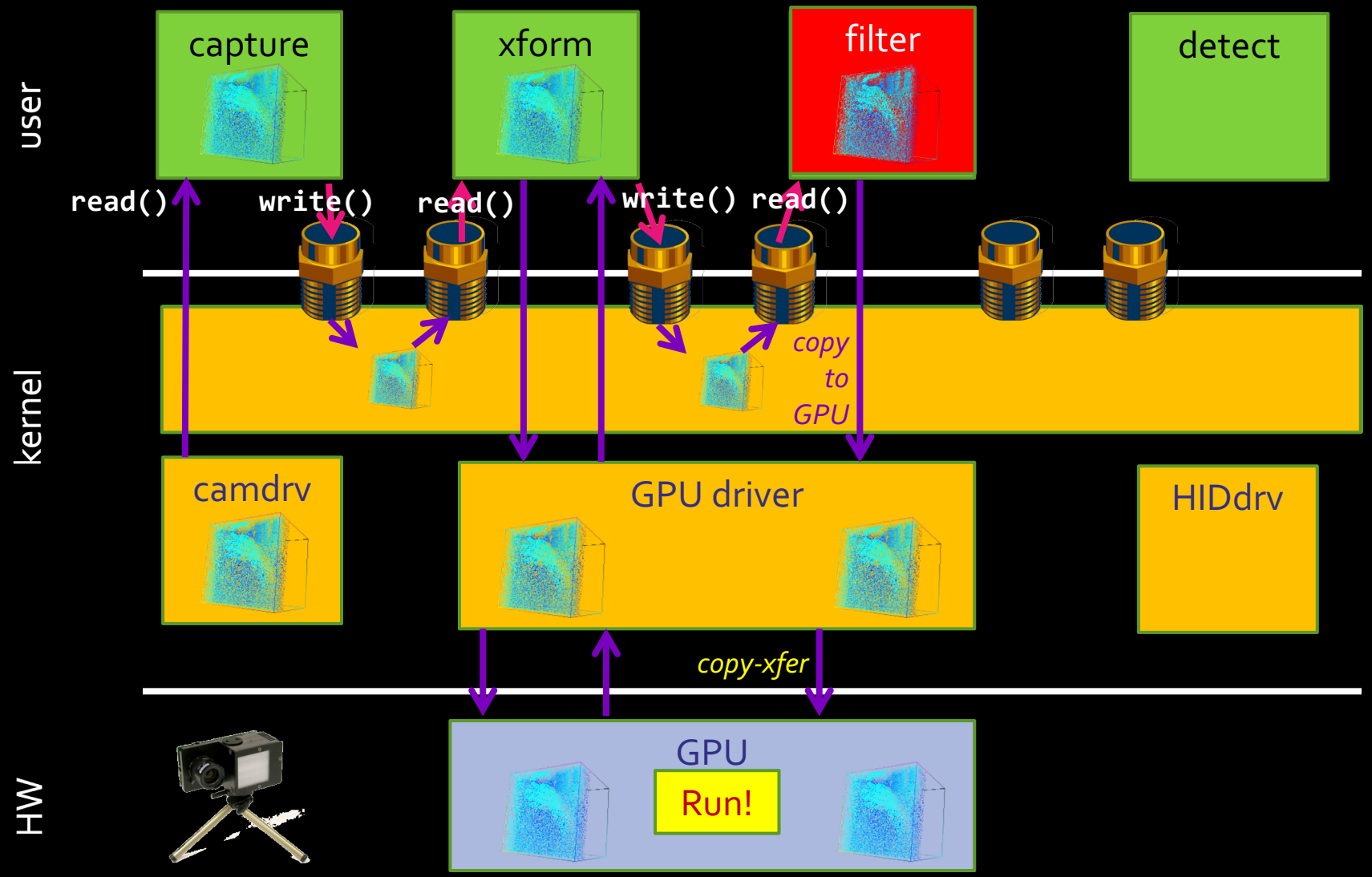

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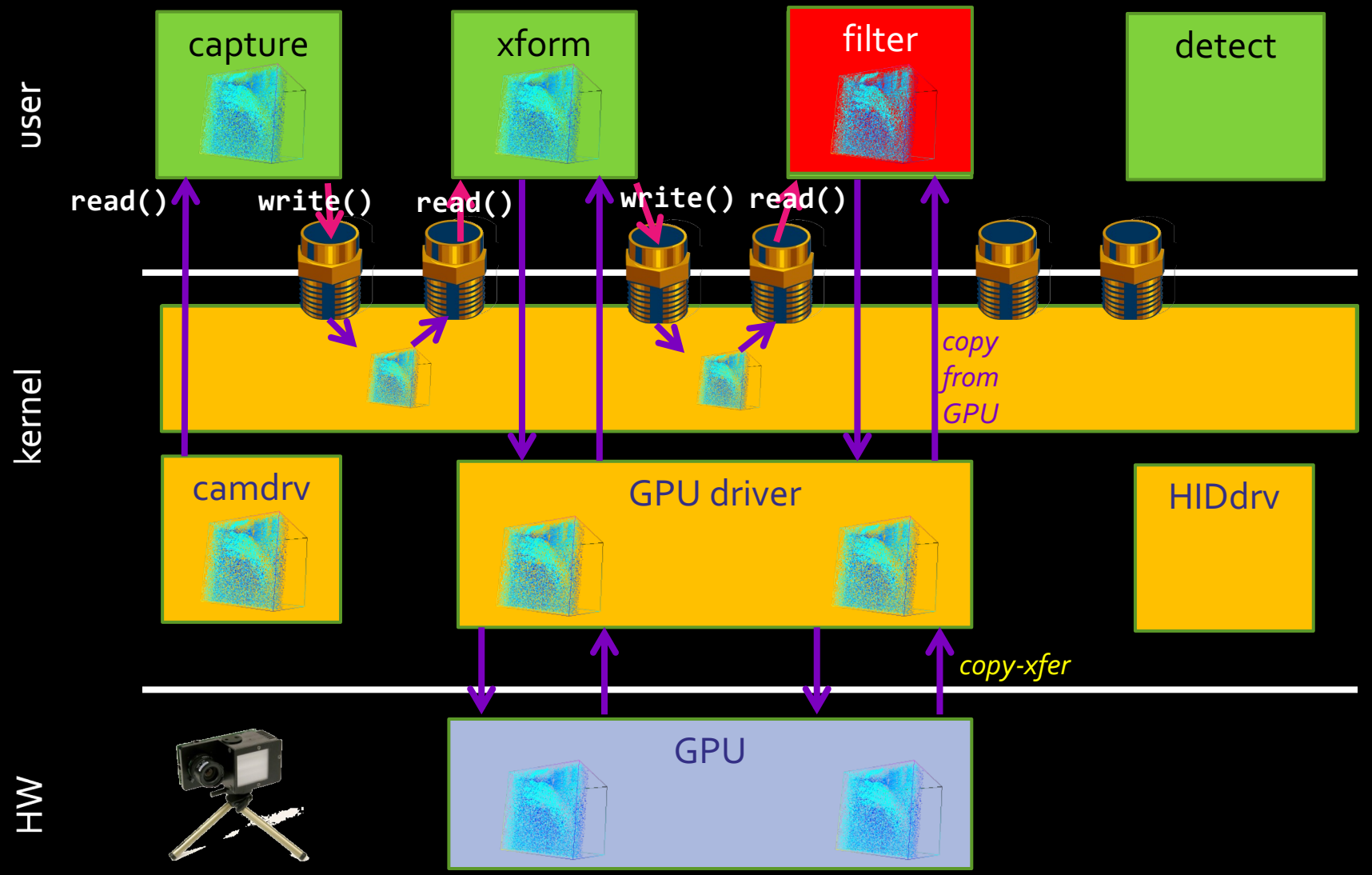

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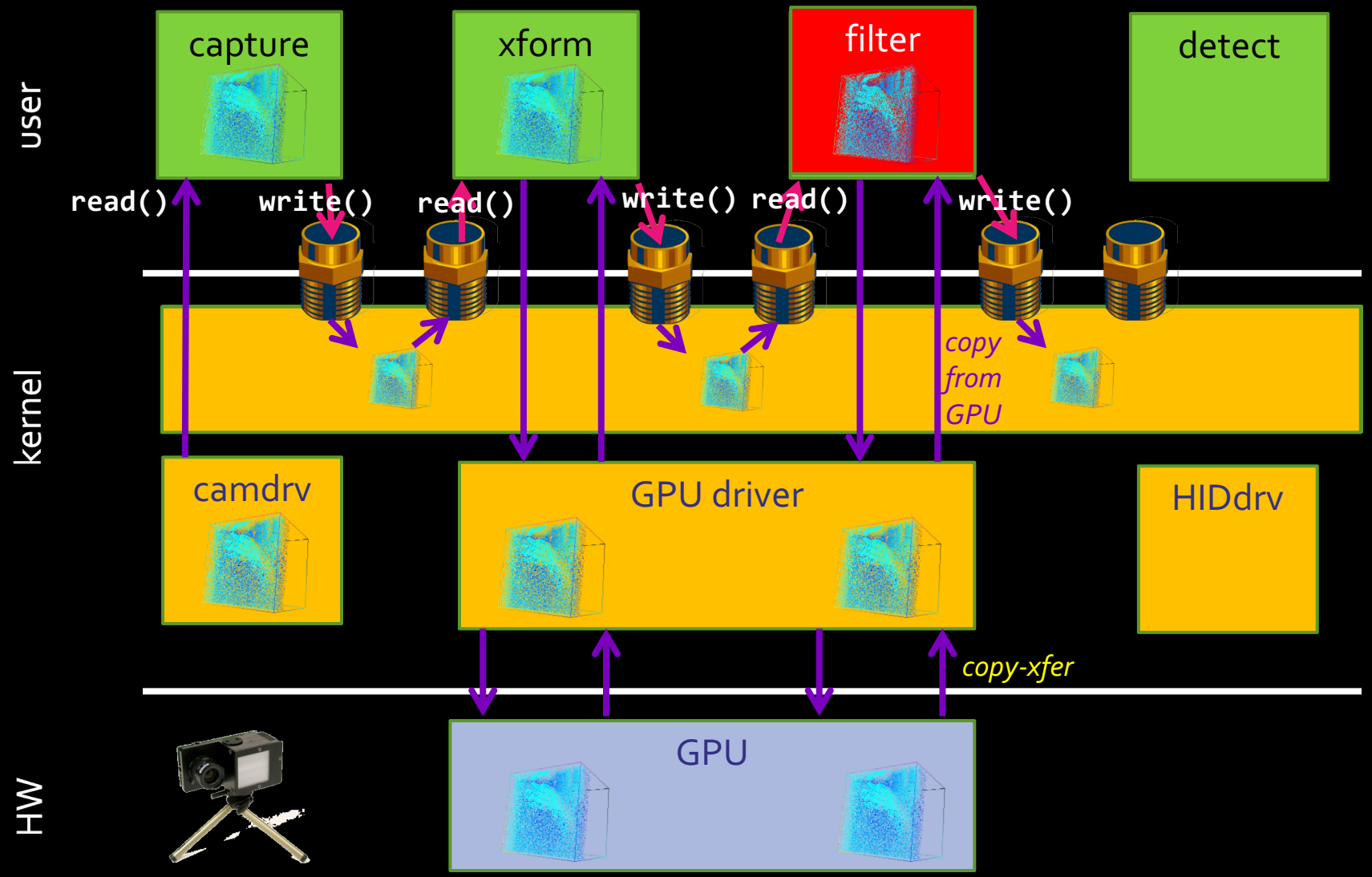

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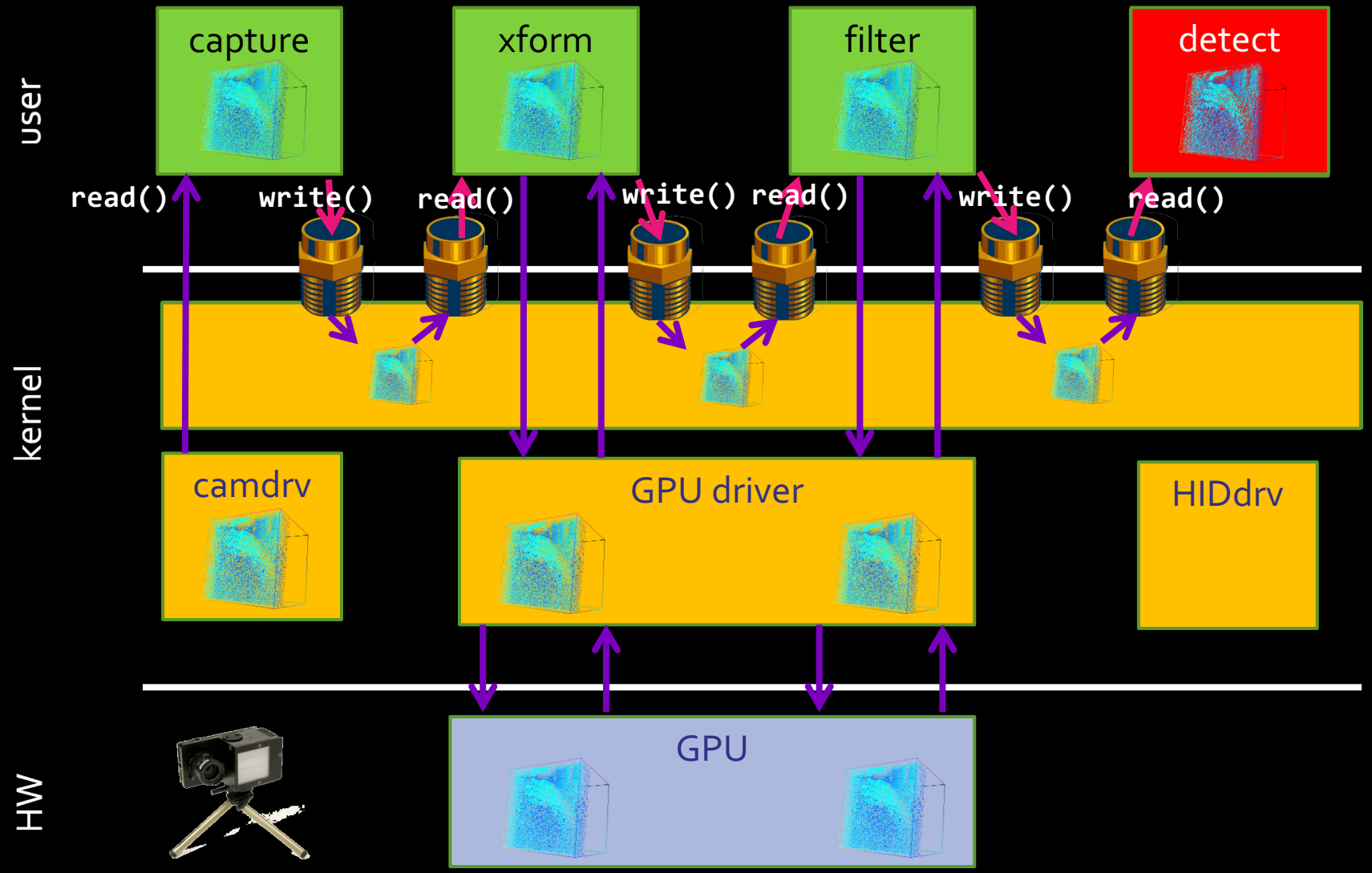

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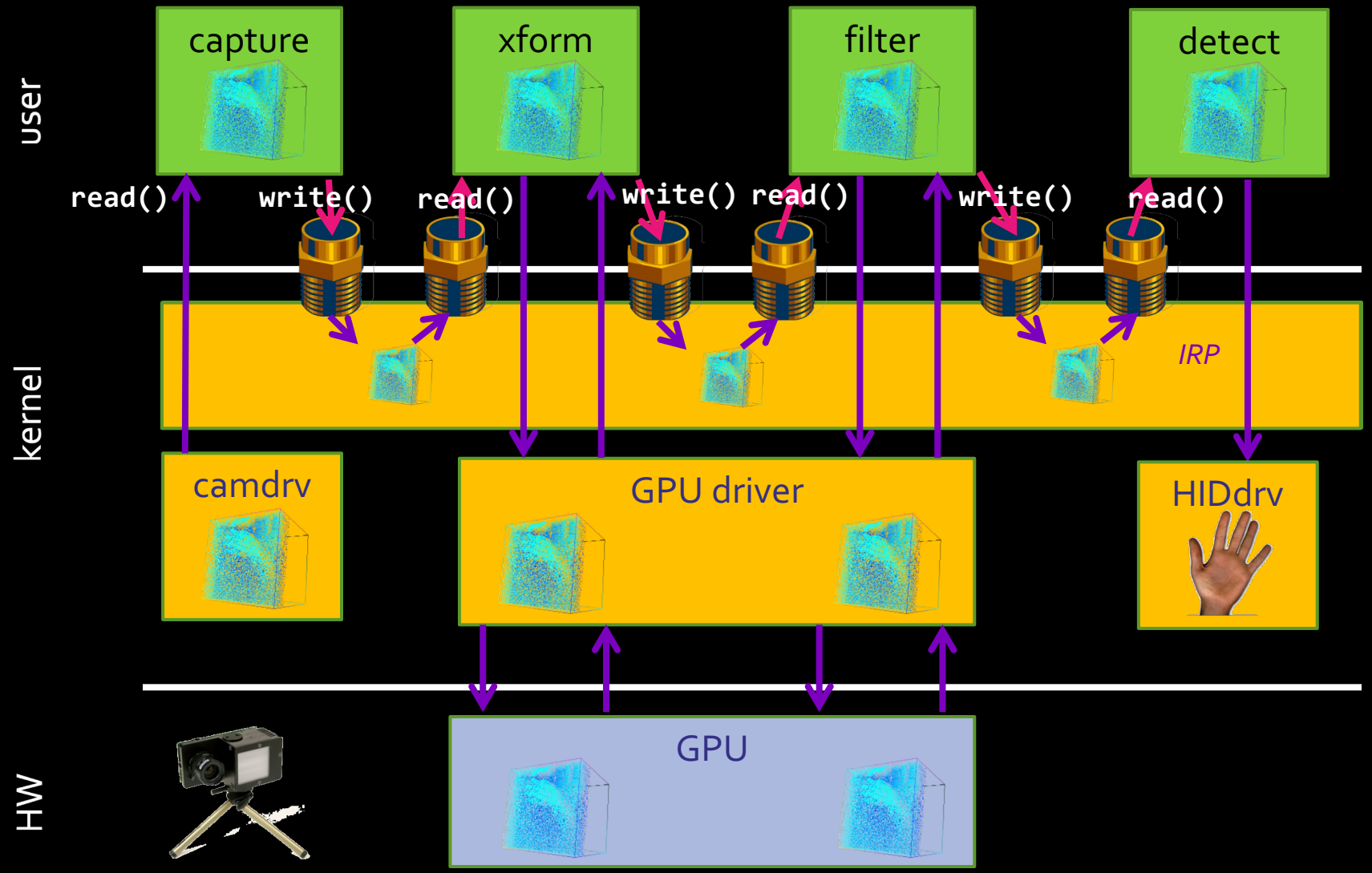

Device-centric APIs considered harmful

```
Matrix
gemm(Matrix A, Matrix B) {
    copyToGPU(A);
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    invokeGPU();
    Matrix C = new Matrix();
    copyFromGPU(C);
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}
```

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What happens if I want the following?

Matrix D = A x B x C

Composed matrix multiplication

```
Matrix
AxBxC(Matrix A, B, C) {
    Matrix AxB = gemm(A,B);
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Composed matrix multiplication

AxB copied from GPU memory…

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…only to be copied right back!

What if I have many GPUs?

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What if I have many GPUs?

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Matrix
gemm(GPU dev,Matrix A, Matrix B) {
    copyToGPU(dev, A);
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What if I have many GPUs?

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Matrix
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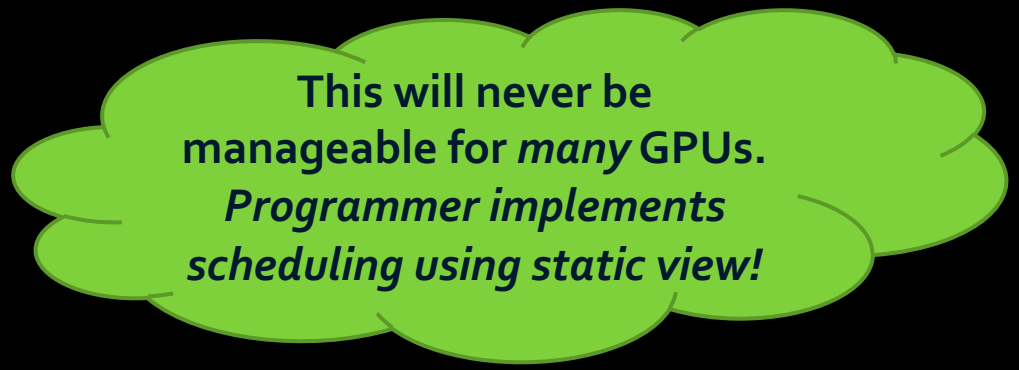


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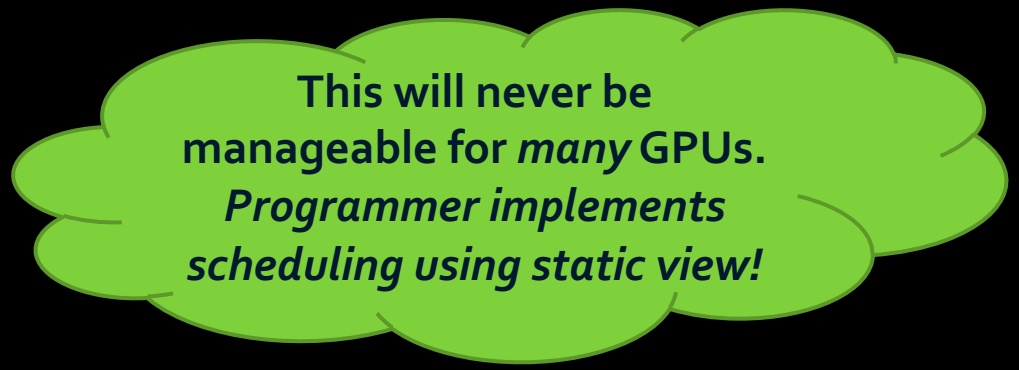


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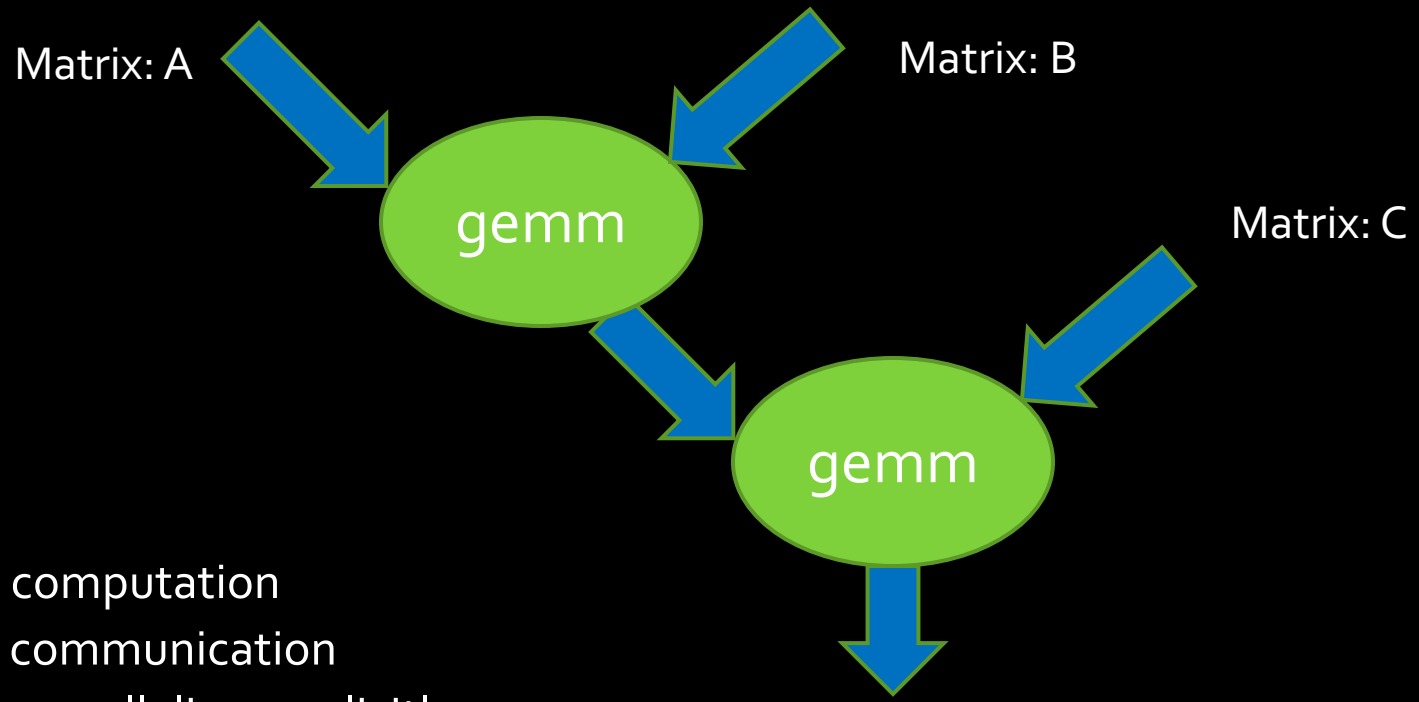
Why don't we have this problem with CPUs?

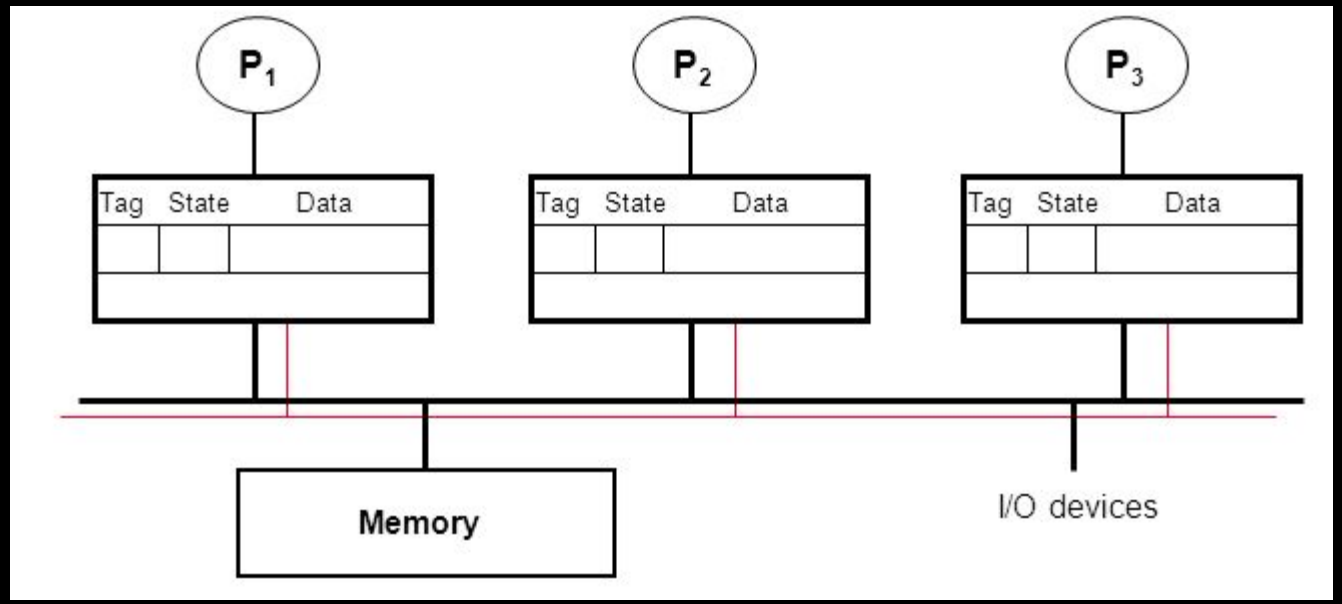
Dataflow: a better abstraction



- nodes → computation
- edges → communication
- Expresses parallelism explicitly
- Minimal specification of data movement: runtime does it.
- asynchrony is a runtime concern (not programmer concern)
- No specification of compute→device mapping: like threads!

Advanced Topic: GPU Coherence

Review: Cache Coherence



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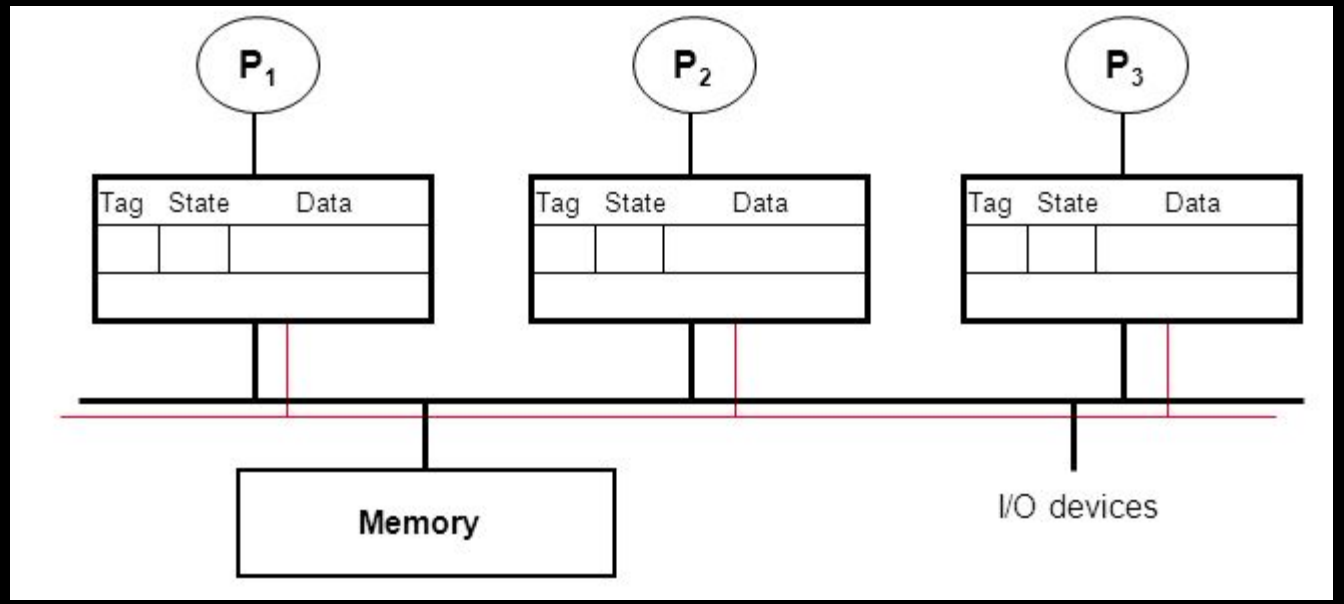

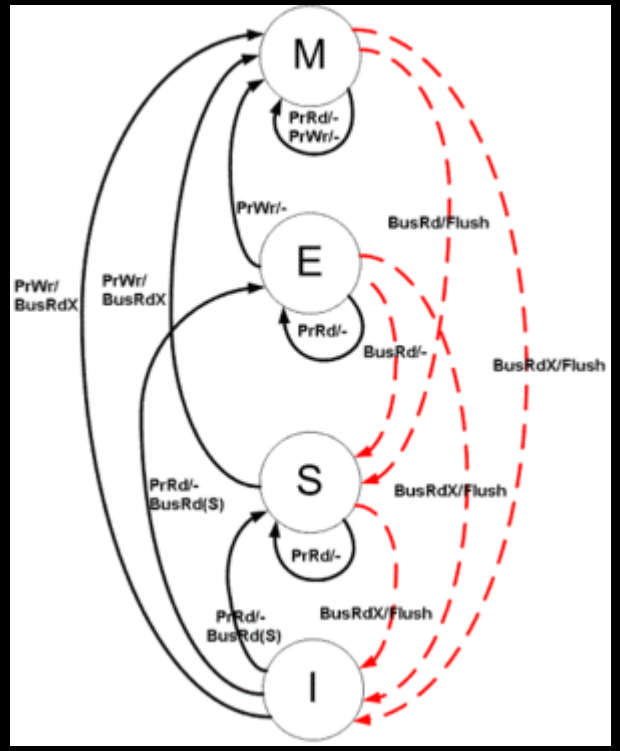

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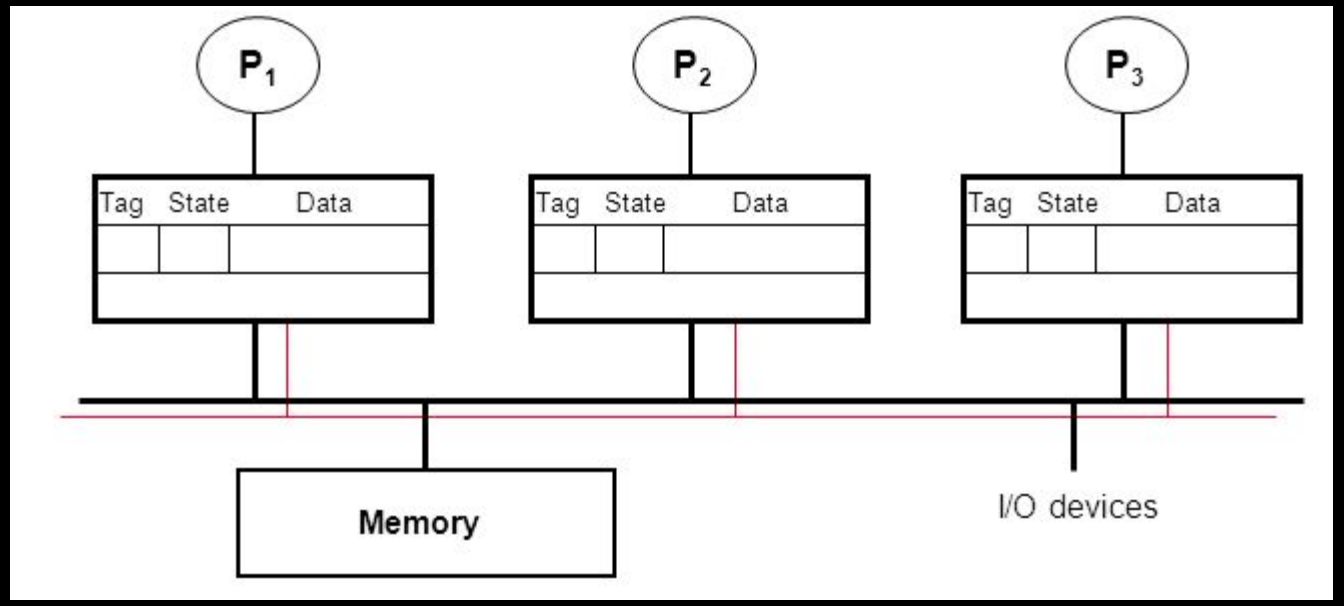
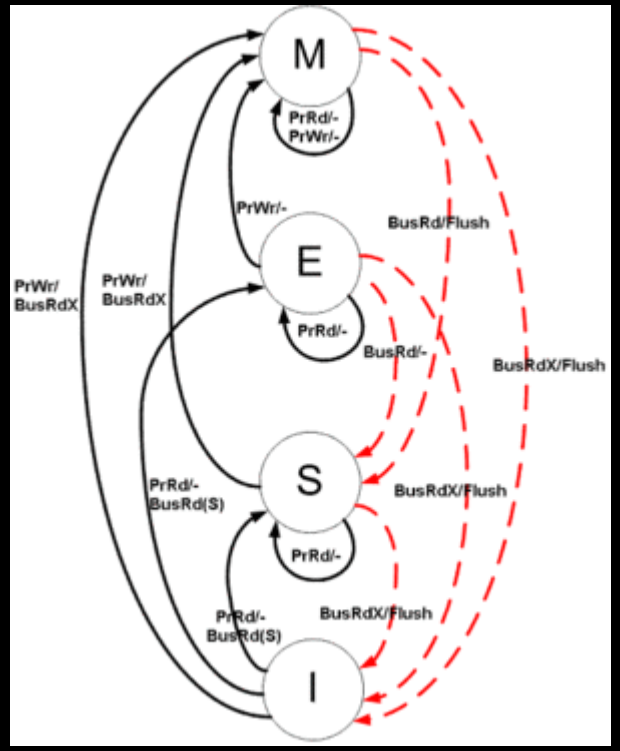


Each cache line has a state (M, E, S, I)



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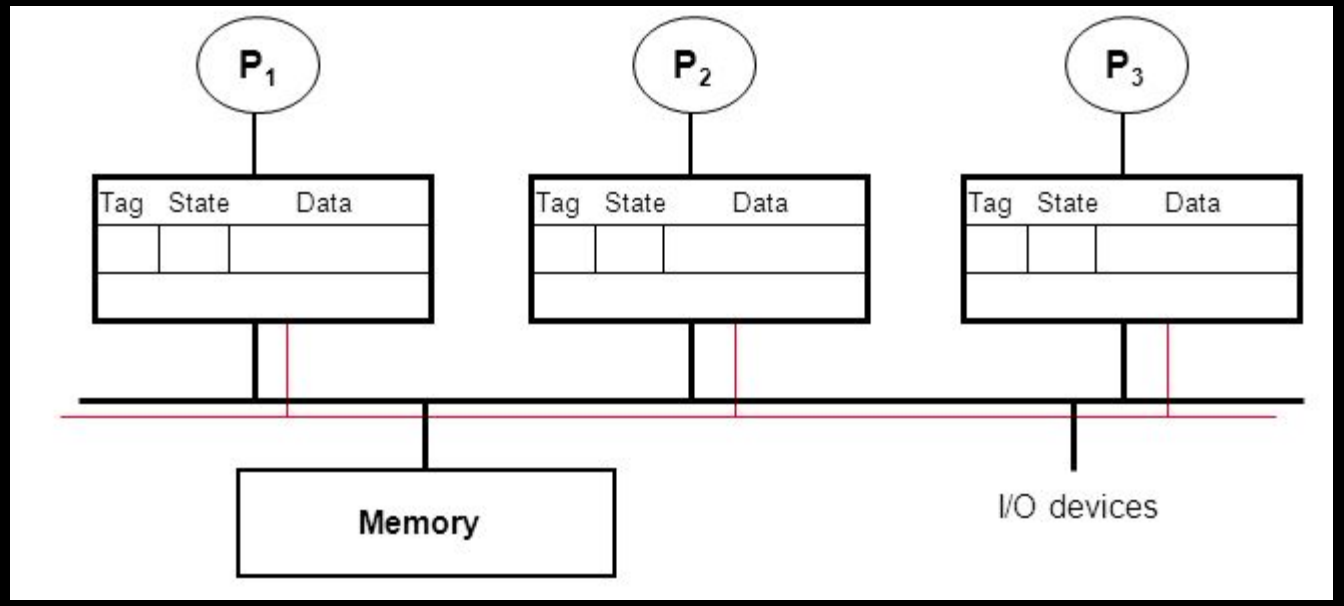

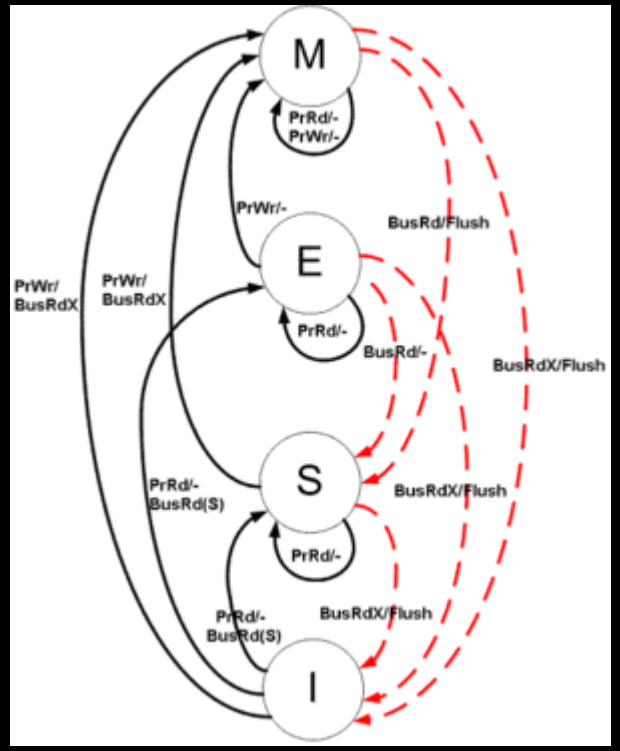

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- Processors "snoop" bus to maintain states

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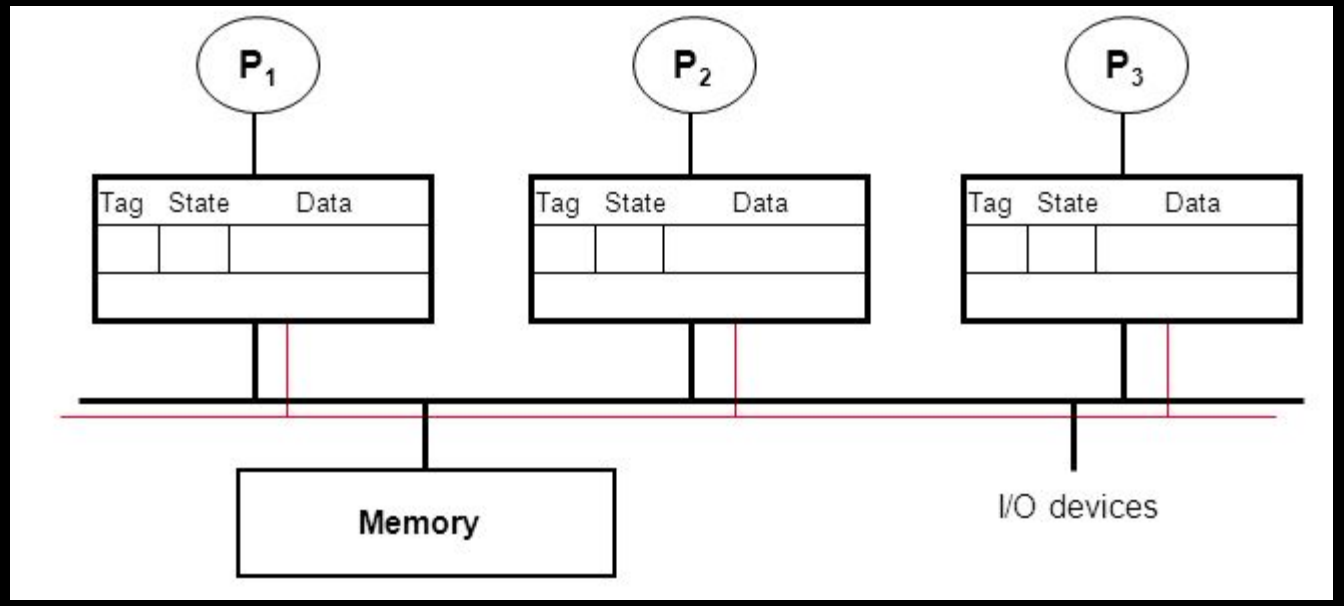
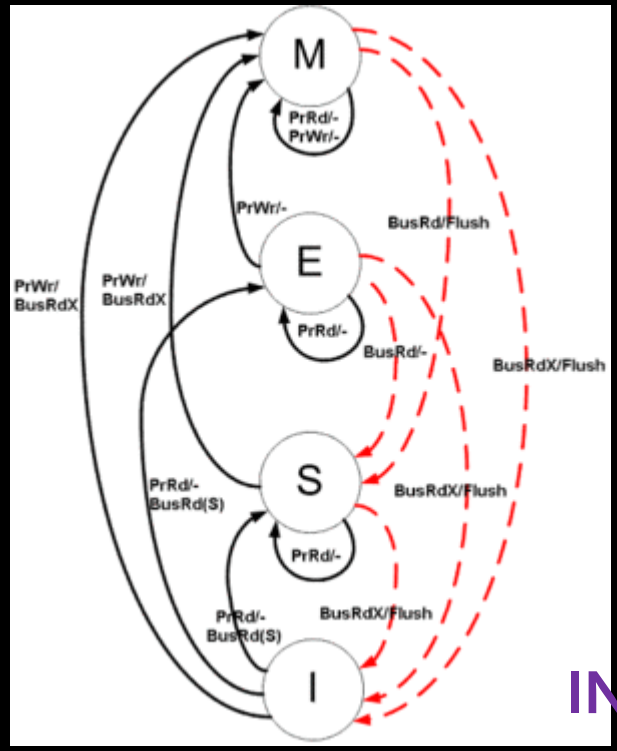


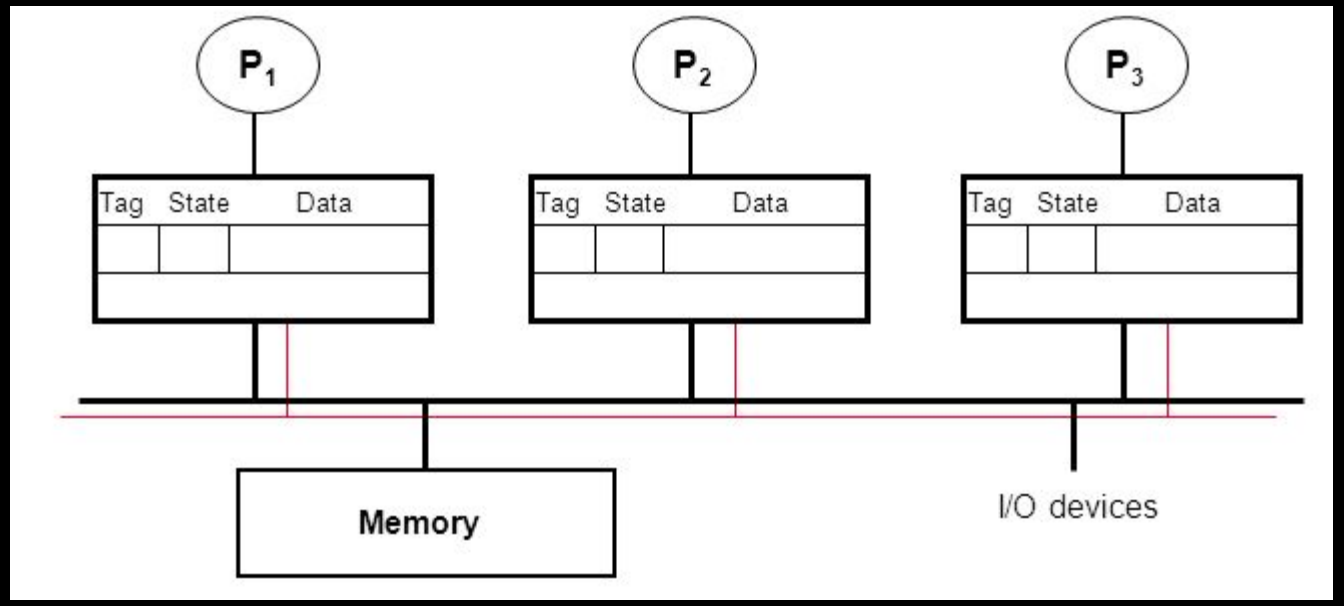


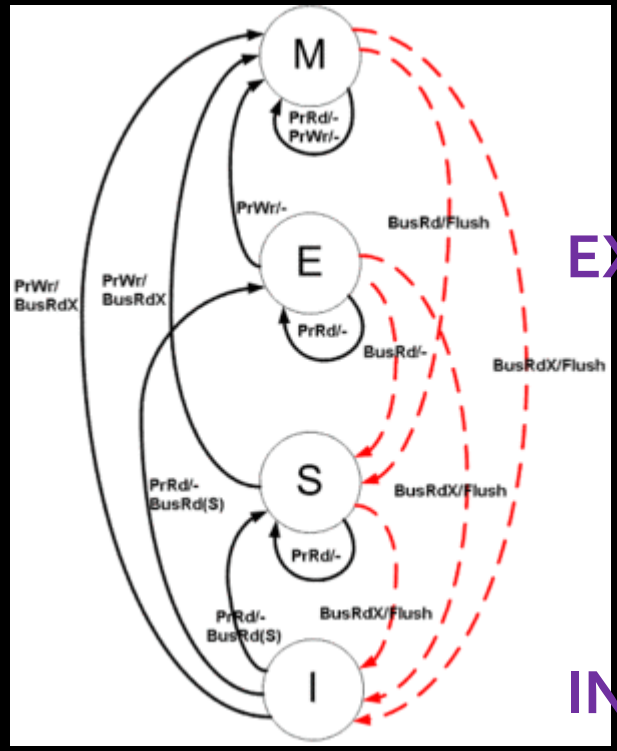
Each cache line has a state (M, E, S, I)

- Processors "snoop" bus to maintain states
- Initially → 'I' → Invalid

INVALID

Review: Cache Coherence





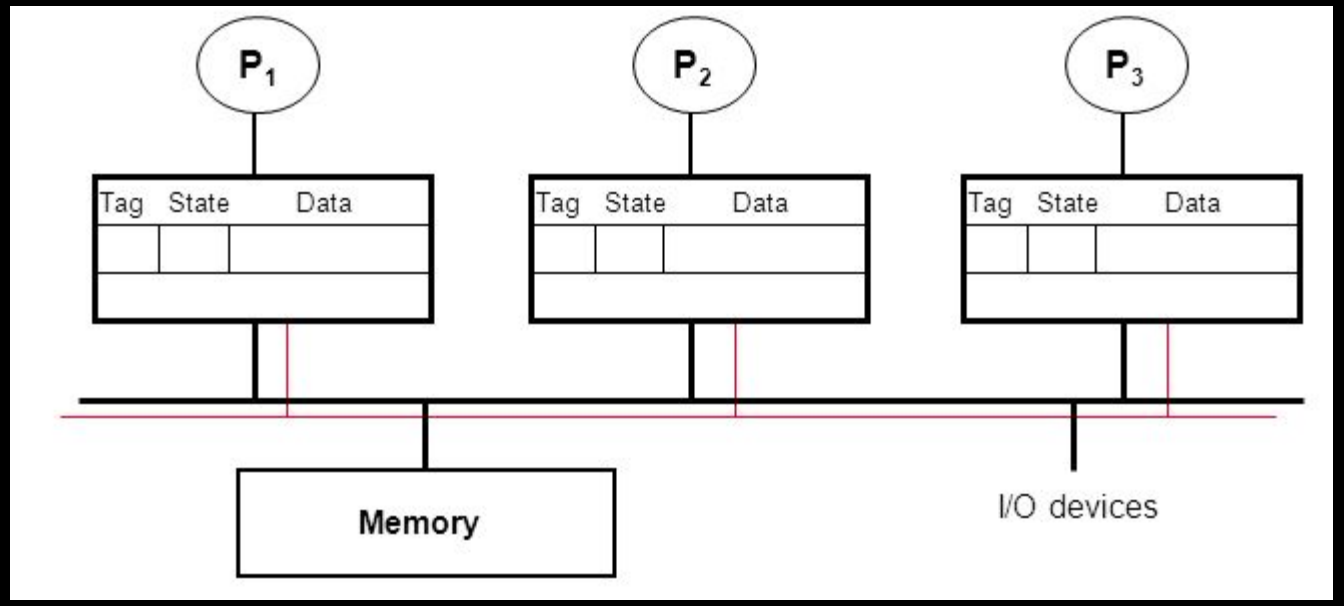
EXCLUSIVE

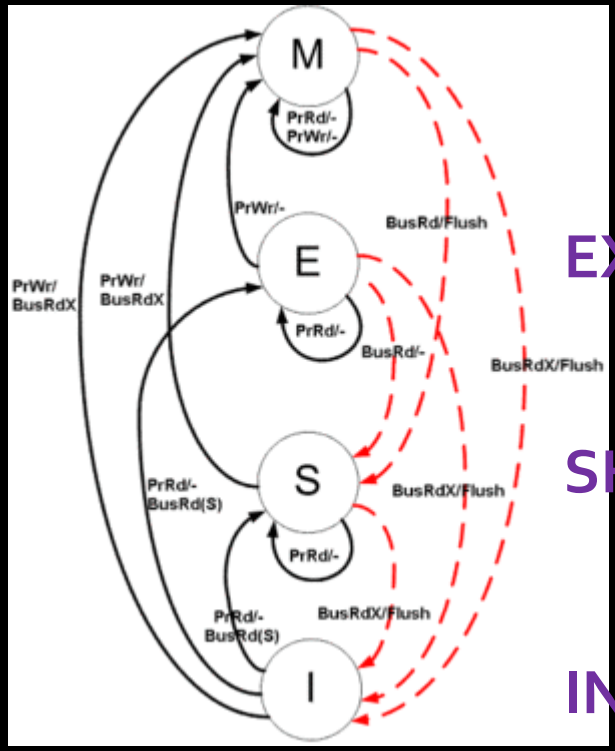
INVALID

Each cache line has a state (M, E, S, I)

- Processors "snoop" bus to maintain states
- Initially → 'I' → Invalid
- Read one → 'E' → exclusive

Review: Cache Coherence





EXCLUSIVE

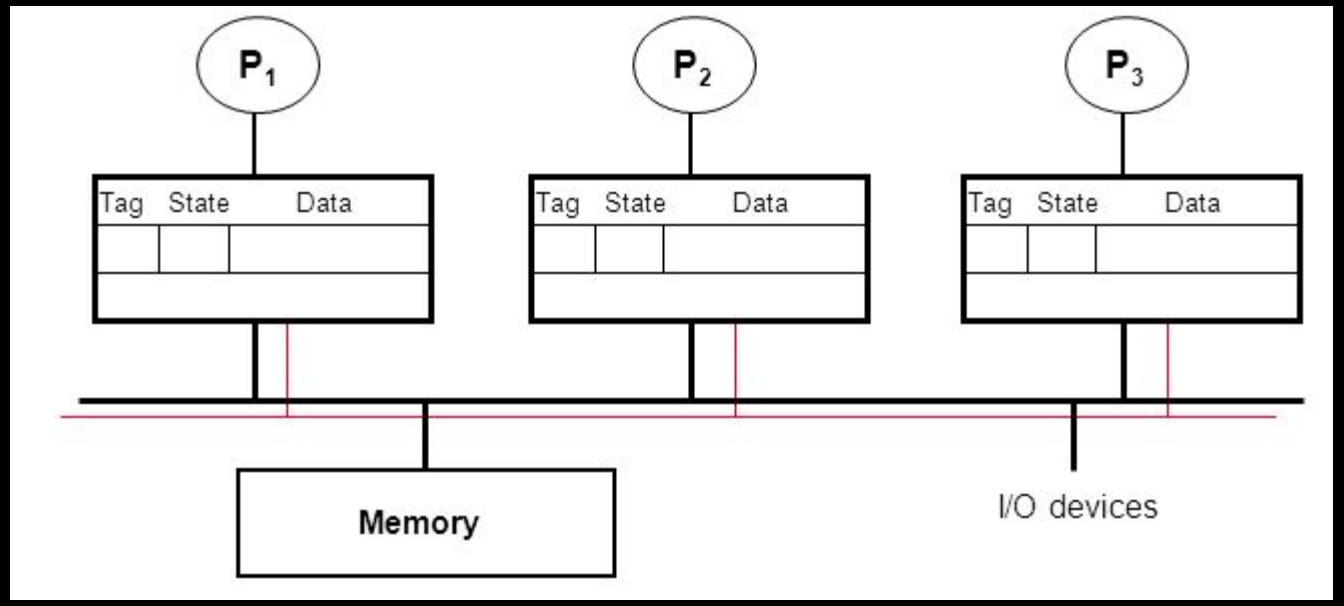
SHARED

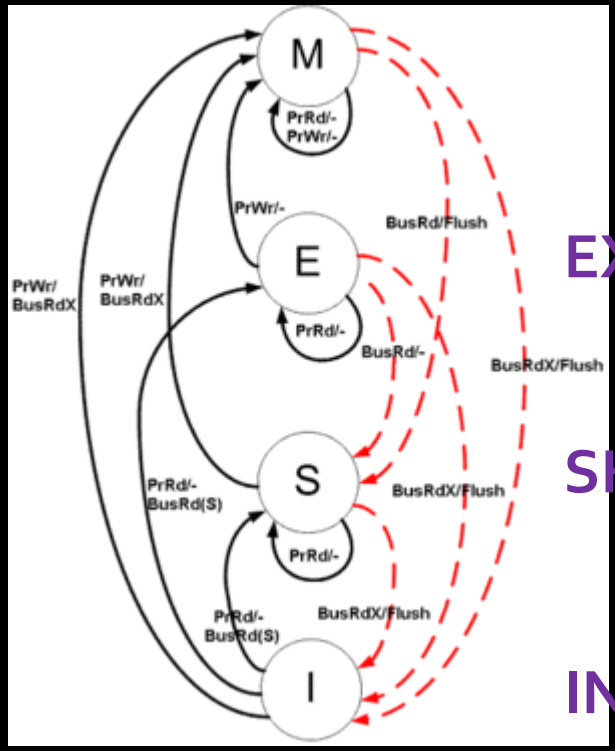
INVALID

Each cache line has a state (M, E, S, I)

- Processors "snoop" bus to maintain states
- Initially → 'I' → Invalid
- Read one → 'E' → exclusive
- Reads → 'S' → multiple copies possible

Review: Cache Coherence





EXCLUSIVE

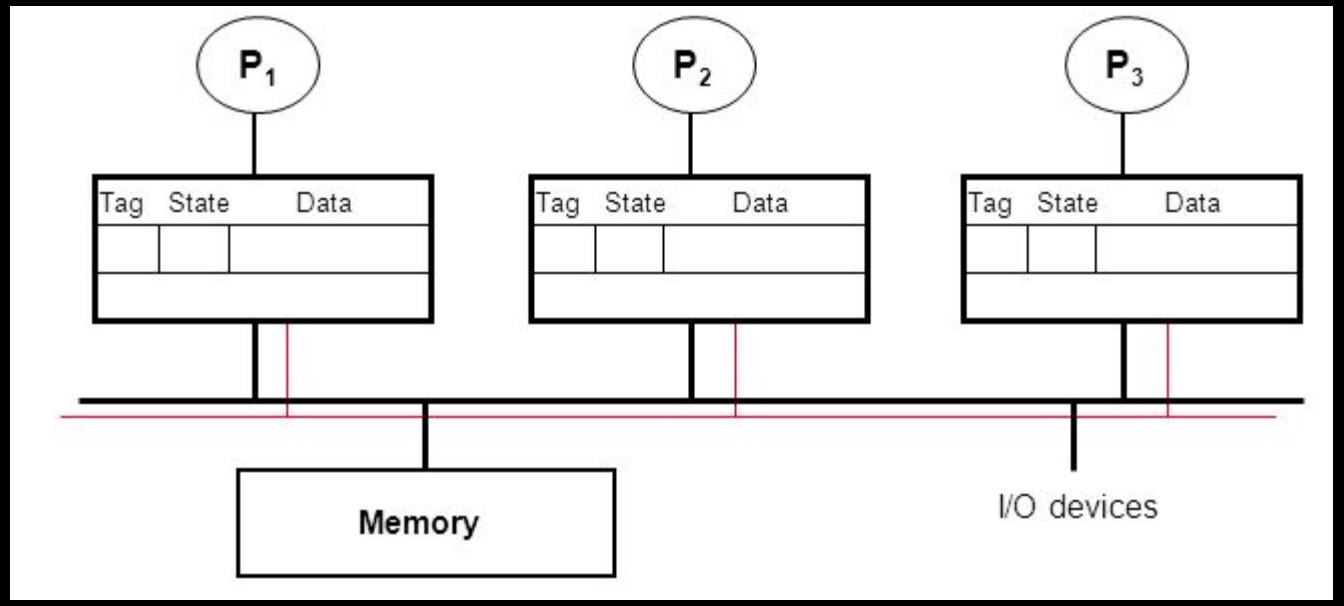
SHARED

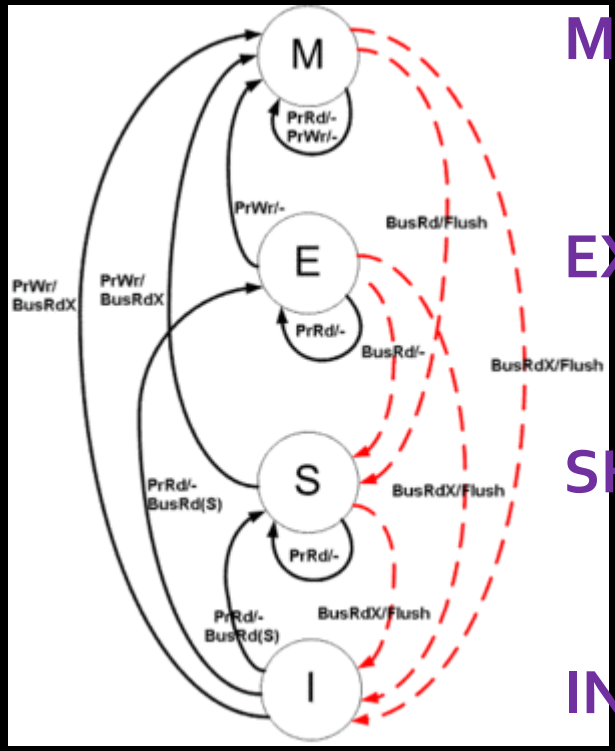
INVALID

Each cache line has a state (M, E, S, I)

- Processors "snoop" bus to maintain states
- Initially → 'I' → Invalid
- Read one → 'E' → exclusive
- Reads → 'S' → multiple copies possible
- Write → 'M' → single copy → lots of cache coherence traffic

Review: Cache Coherence





MODIFIED

EXCLUSIVE

SHARED

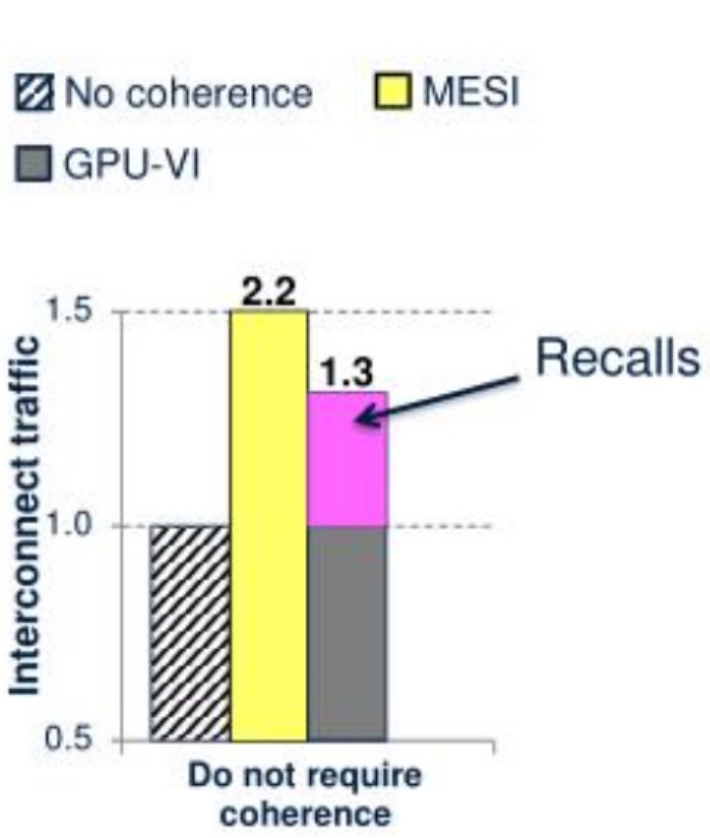
INVALID

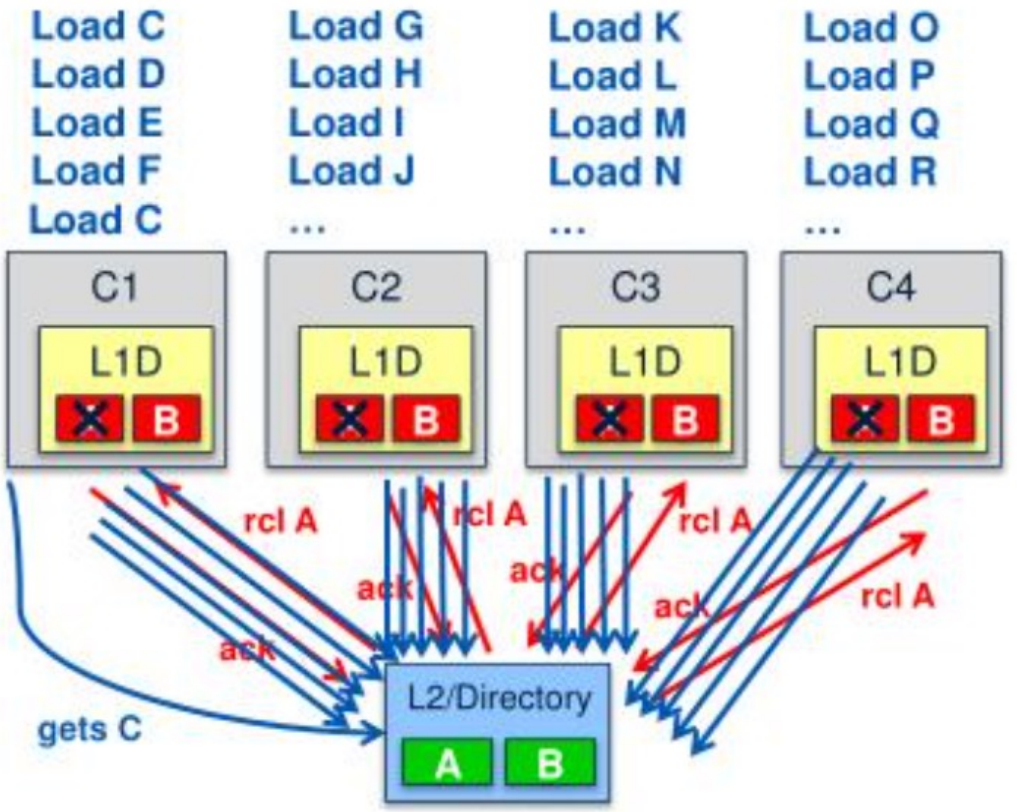
Each cache line has a state (M, E, S, I)

- Processors "snoop" bus to maintain states
- Initially → 'I' → Invalid
- Read one → 'E' → exclusive
- Reads → 'S' → multiple copies possible
- Write → 'M' → single copy → lots of cache coherence traffic

GPU Cache Coherence Challenges

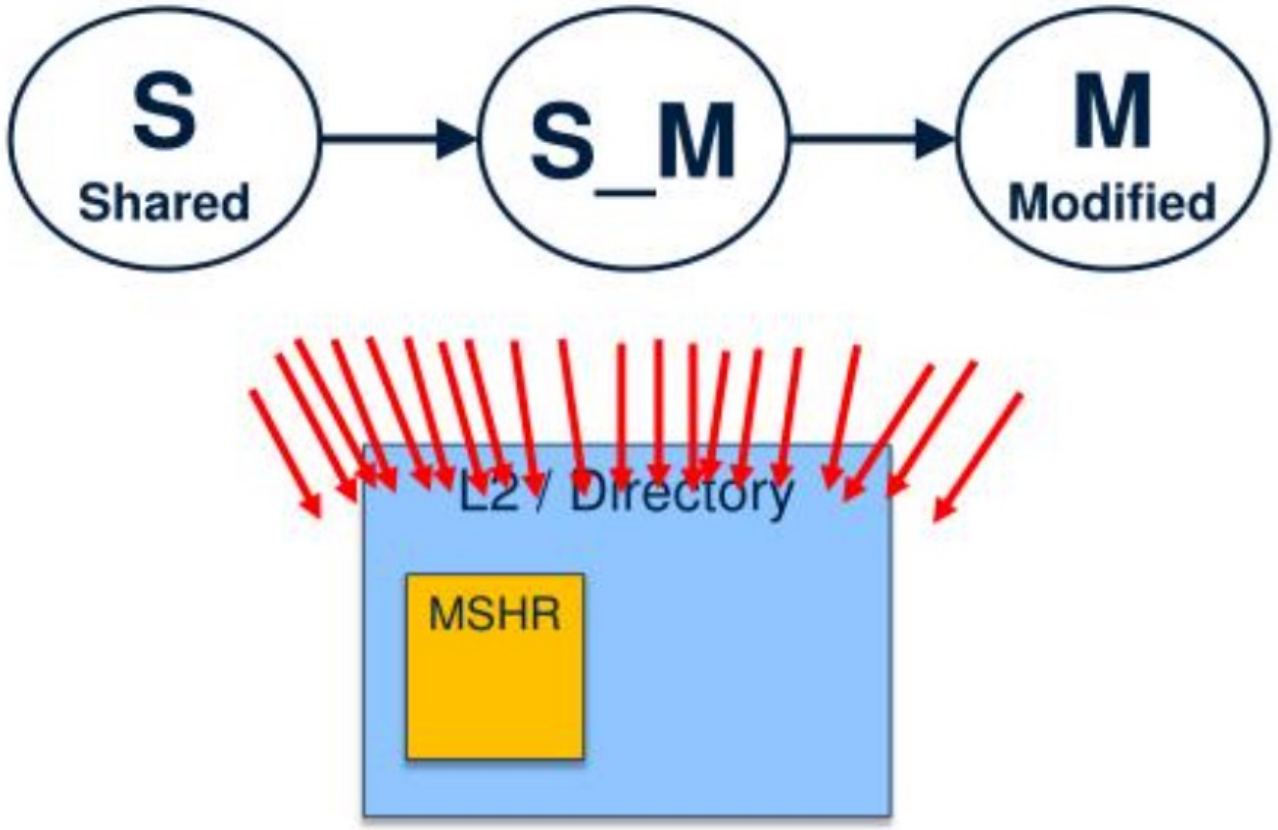
- Challenge 1: Coherence traffic





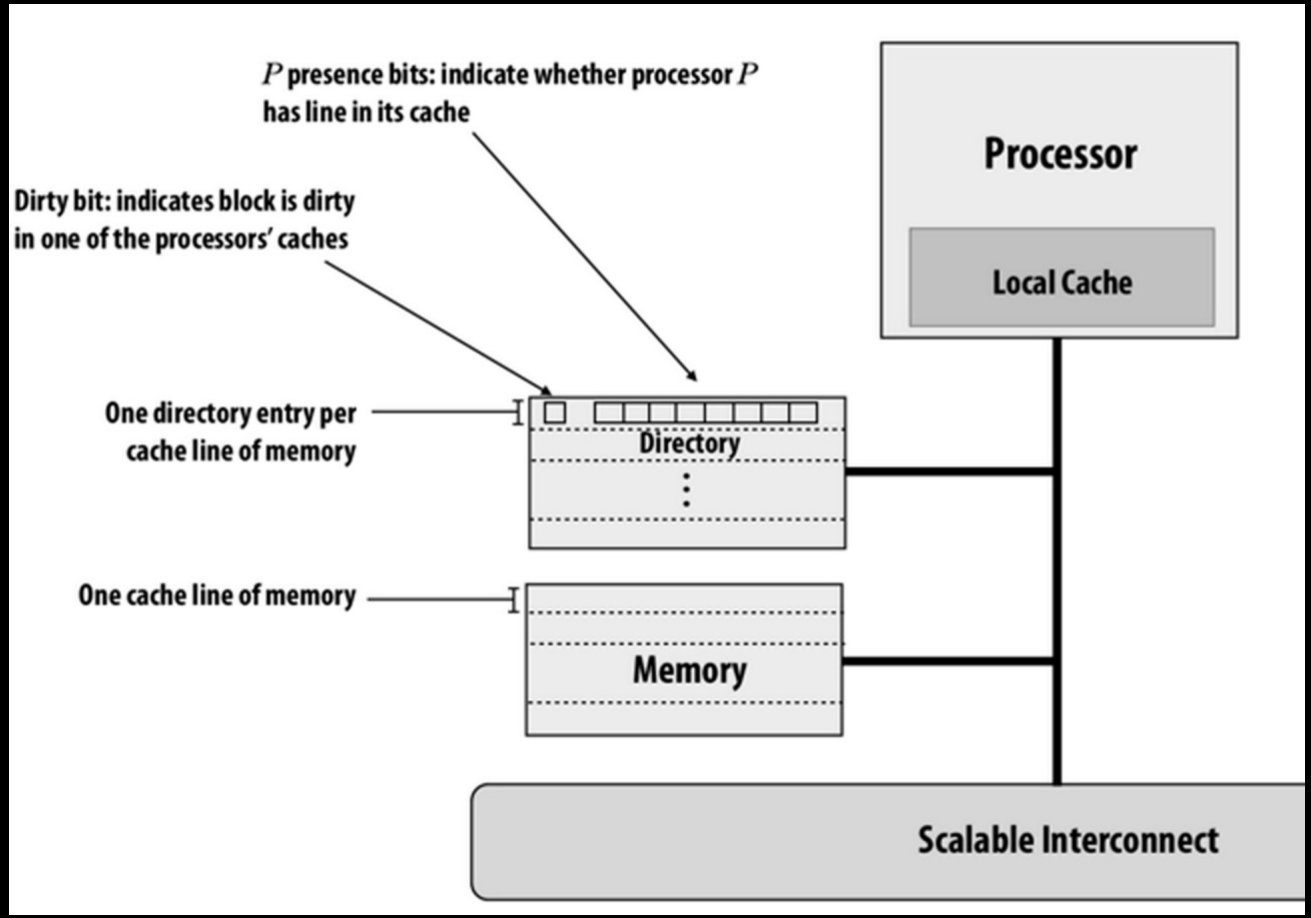
GPU Cache Coherence Challenges

- Challenge 2: Tracking in-flight requests
  - Significant % of L2



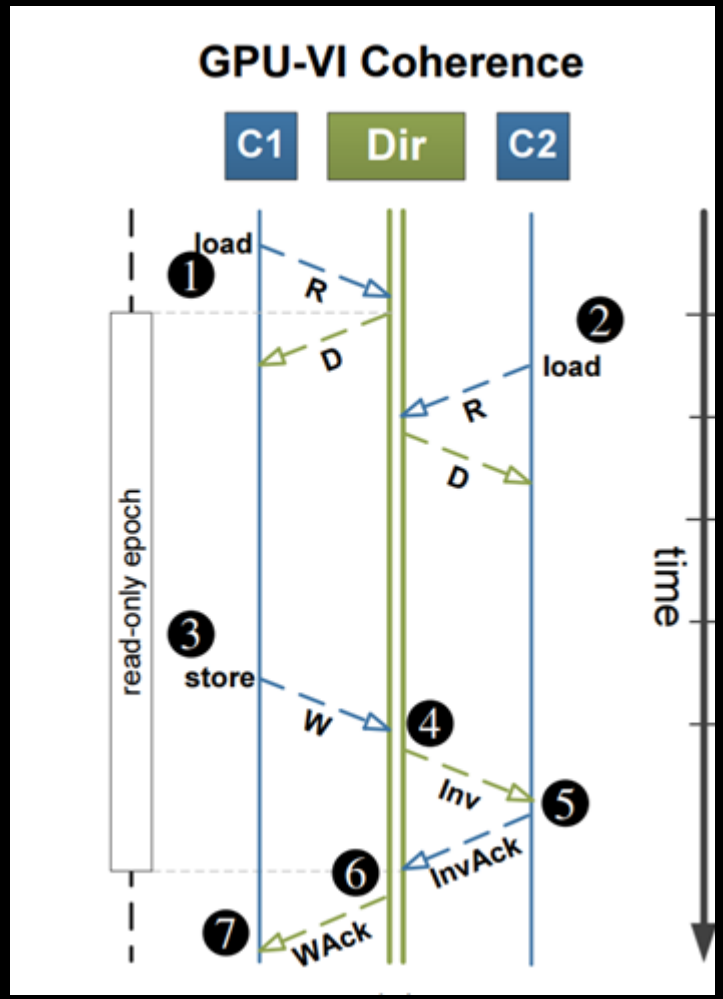
Background: Directory Protocol

- For each block: centralized "directory" for state in caches
- Directory is co-located with some global view of memory
- Requests are no longer seen by everyone
  - ***Writes are serialized through directory***

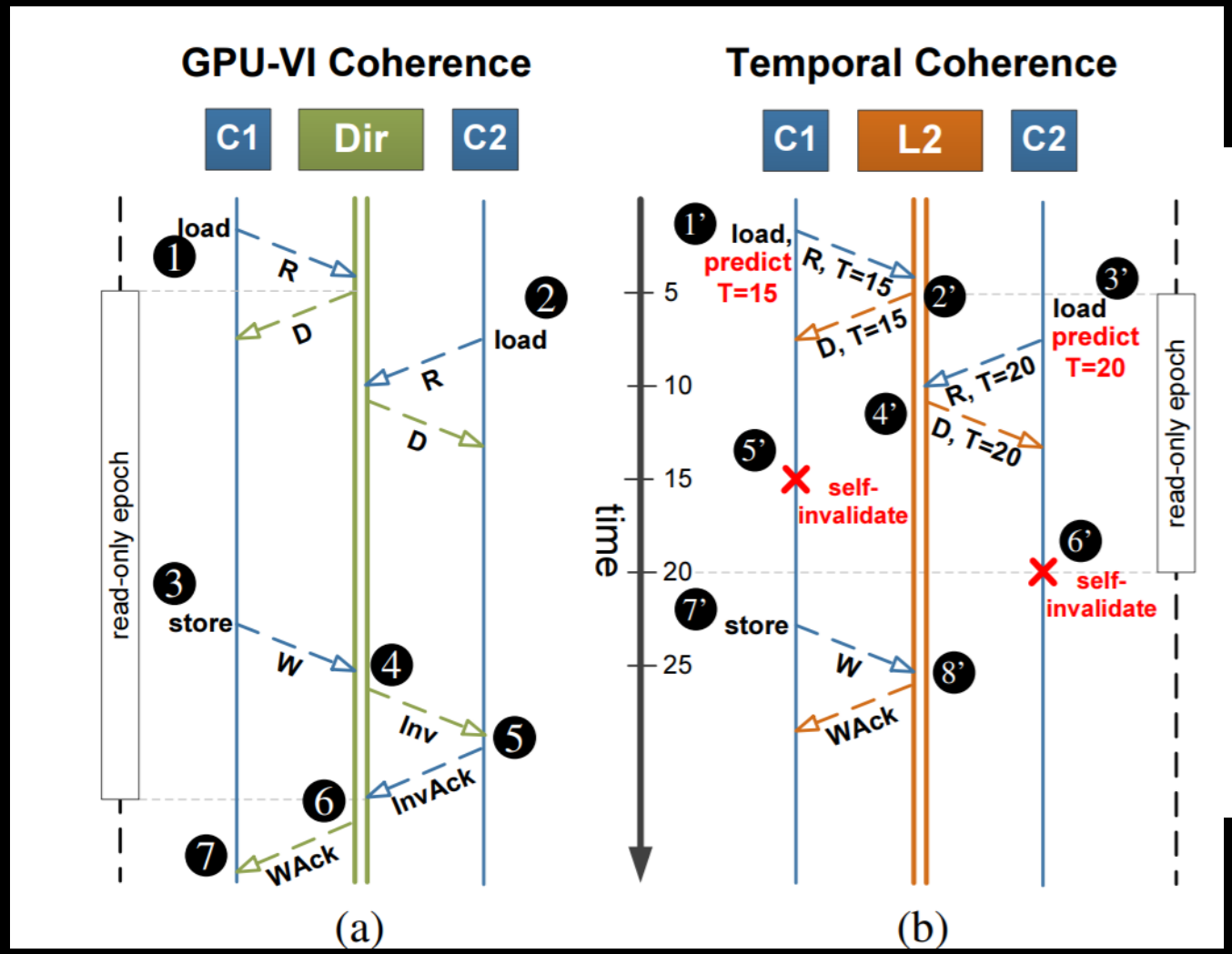


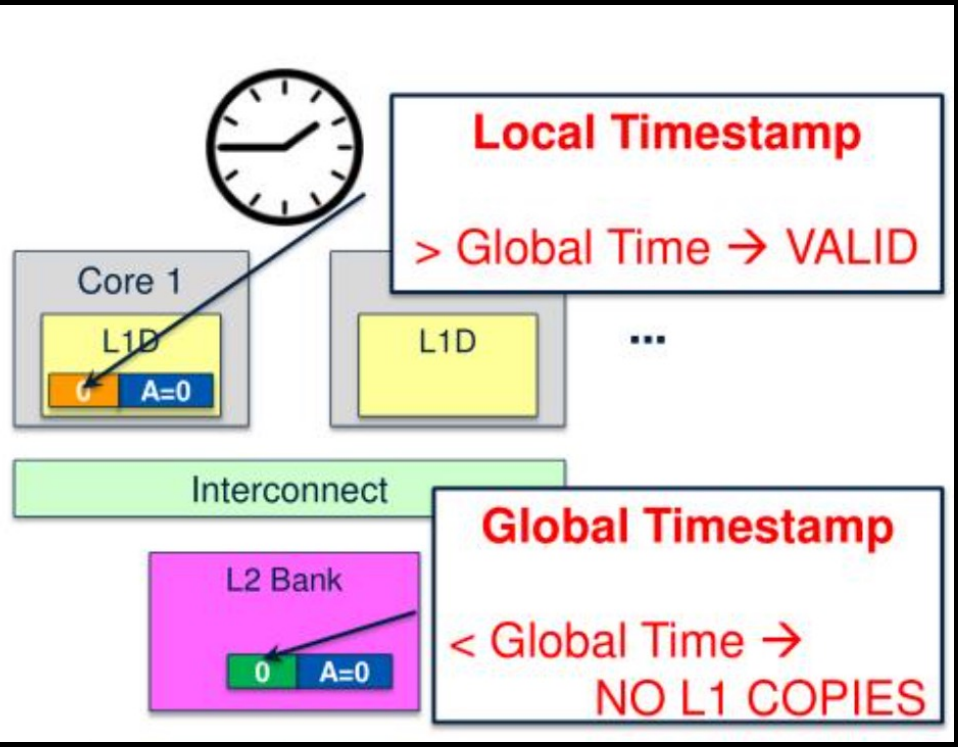
GPU-VI

- Directory-Based
  - Different from snoop-model
  - Global directory metadata at L2
- Two states
  - Valid
  - Invalid
- Writes invalidate other copies



Temporal Coherence (TC)





TC-Strong vs TC-Weak