Parallel Architectures
Parallel Algorithms
CUDA

Chris Rossbach

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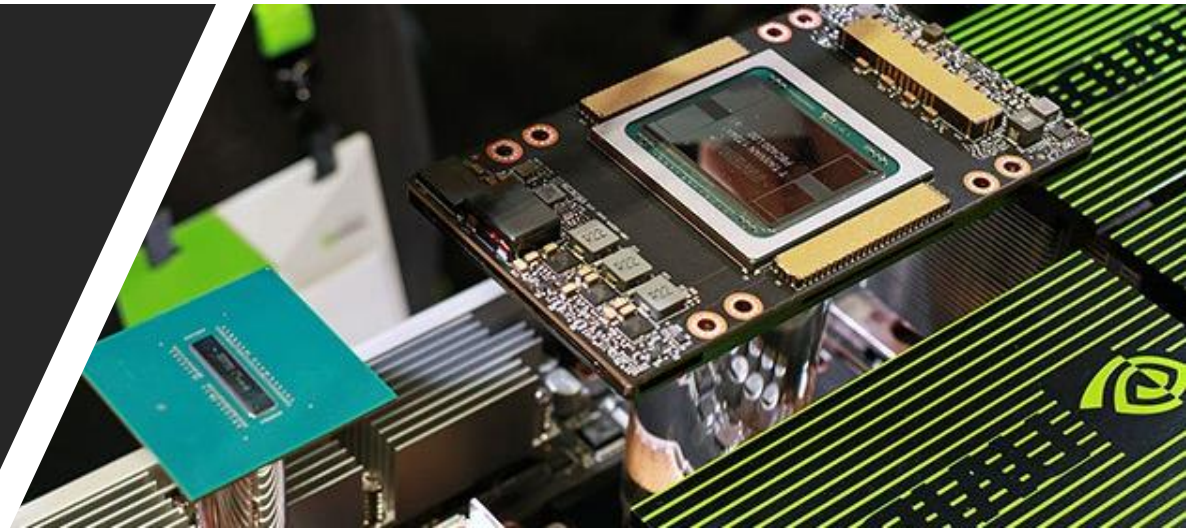
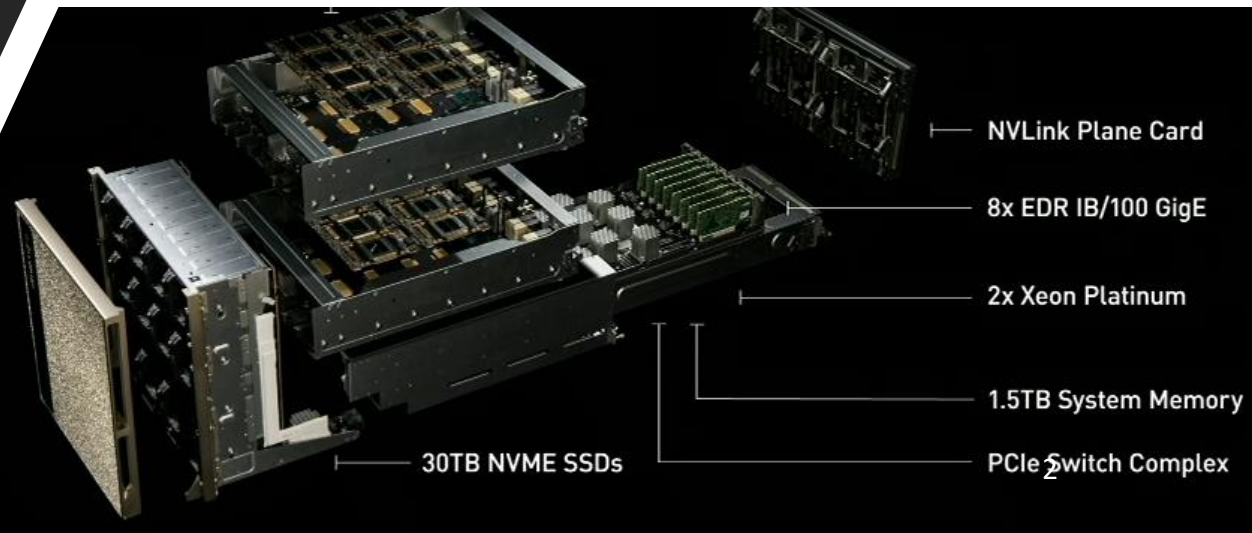
Outline for Today

- Questions?
- Administrivia
  - pedagogical-* machines should be available
- Agenda
  - Parallel Algorithms
  - CUDA

- Acknowledgements: http://developer.download.nvidia.com/compute/developertrainingmaterials/presentations/cuda_language/Introduction_to_CUDA_C.pptx





Faux Quiz Questions

- What is a reduction? A prefix sum? Why are they hard to parallelize and what basic techniques can be used to parallelize them?
- Define flow dependence, output dependence, and anti-dependence: give an example of each. Why/how do compilers use them to detect loop-independent vs loop-carried dependences?
- What is the difference between a thread-block and a warp?
- How/Why must programmers copy data back and forth to a GPU?
- What is “shared memory” in CUDA? Describe a setting in which it might be useful.
- CUDA kernels have implicit barrier synchronization. Why is __syncthreads() necessary in light of this fact?
- How might one implement locks on a GPU?
- What ordering guarantees does a GPU provide across different hardware threads’ access to a single memory location? To two disjoint locations?
- When is it safe for one GPU thread to wait (e.g. by spinning) for another?

Review: what is a vector processor?

```
# C code
for (i=0; i<64; i++)
 C[i] = A[i] + B[i];

# Scalar Code
   LI     R4, 64
loop:
   L.D    F0, 0(R1)
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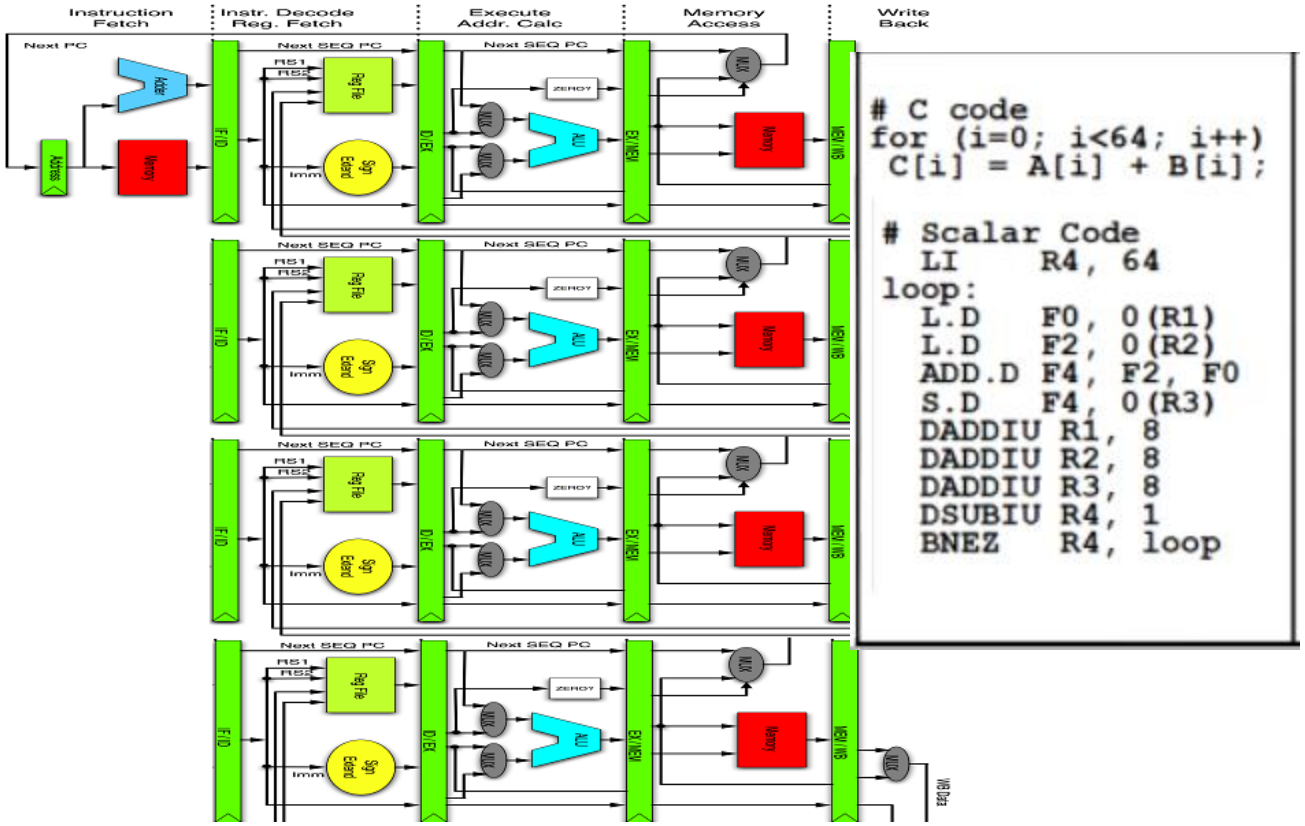


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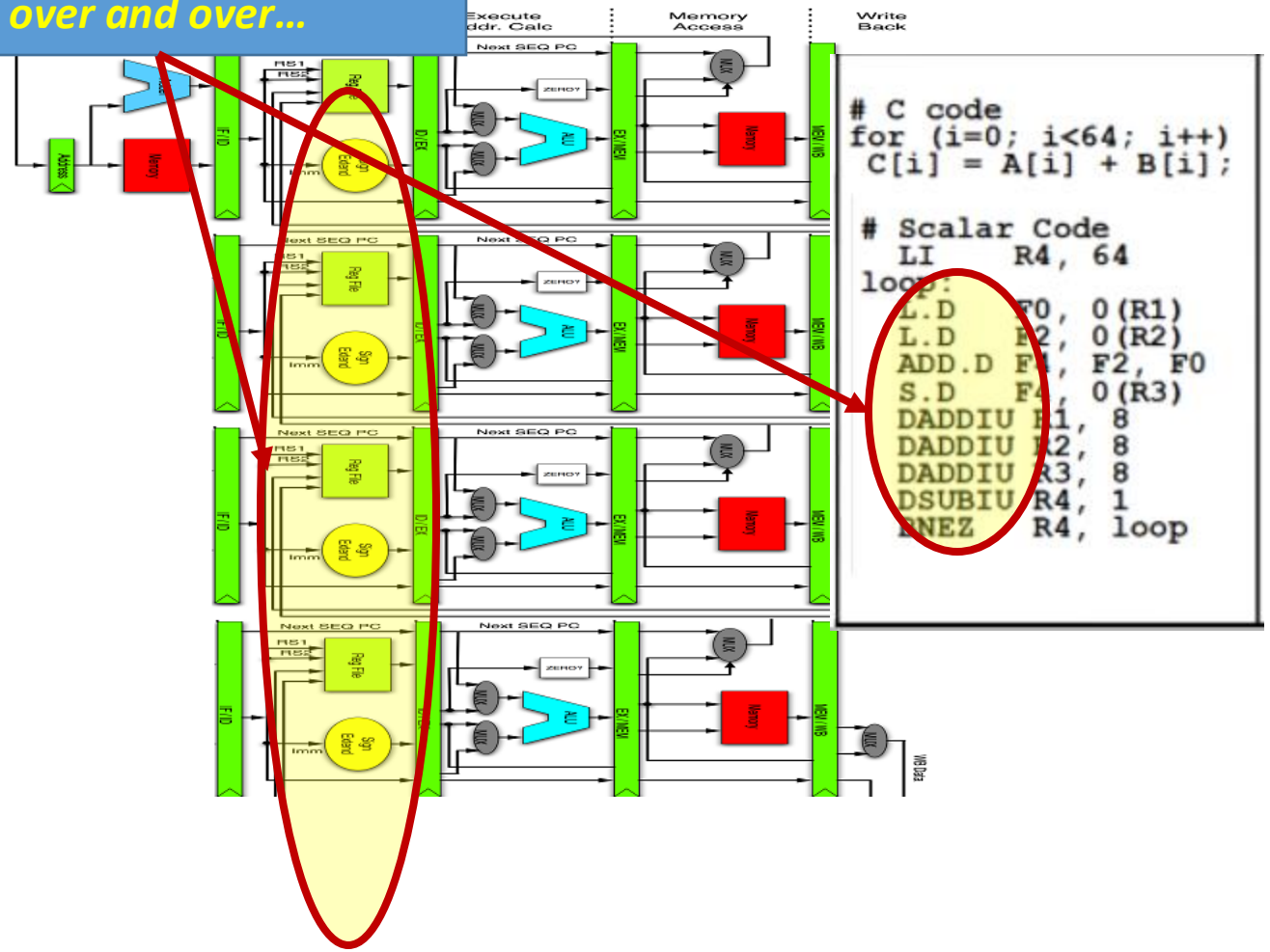
Dont decode same instruction over and over…



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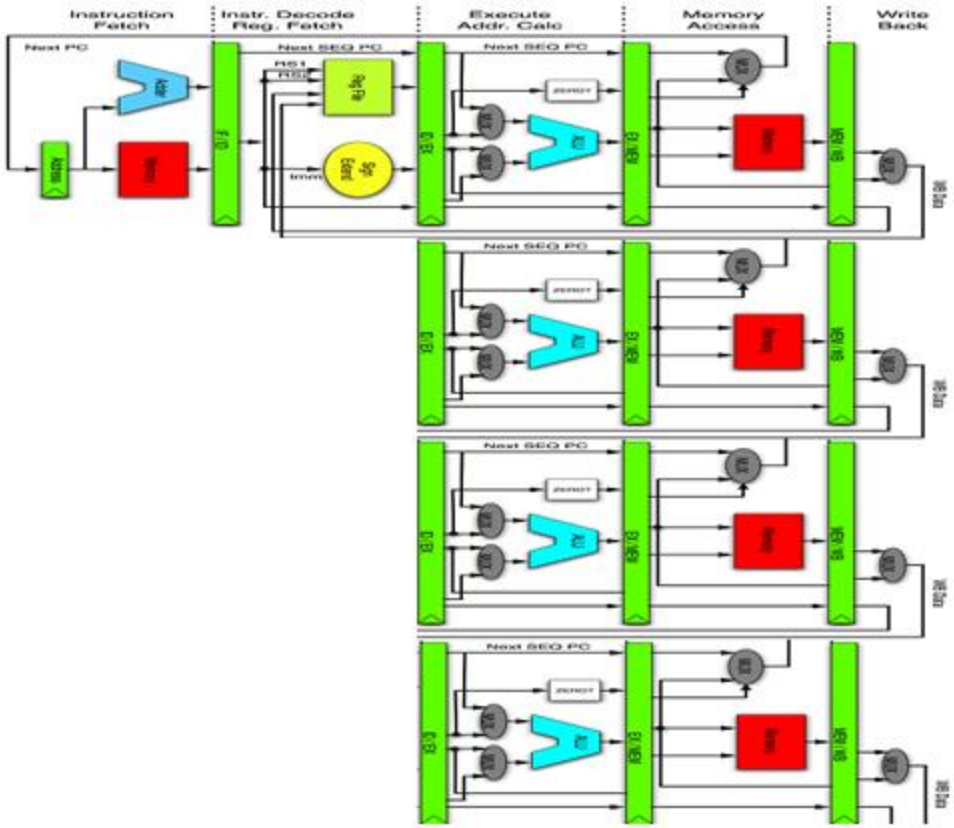

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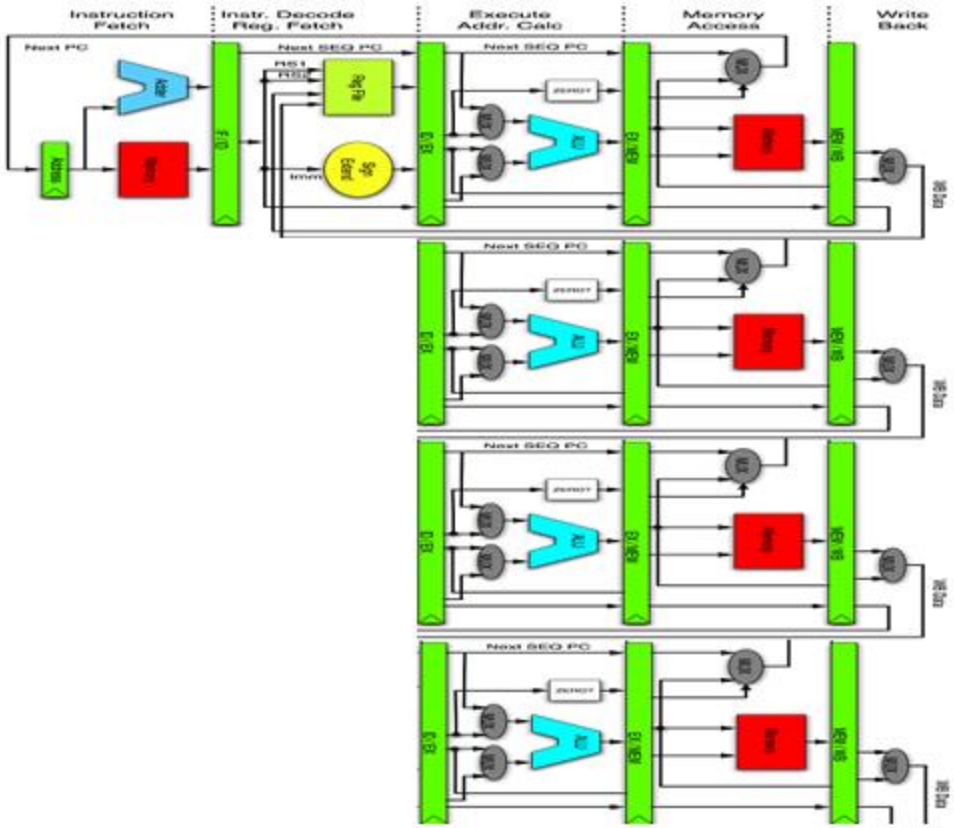


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# Vector Code
  LI     VLR, 64
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  ADDV.D V3, V1, V2
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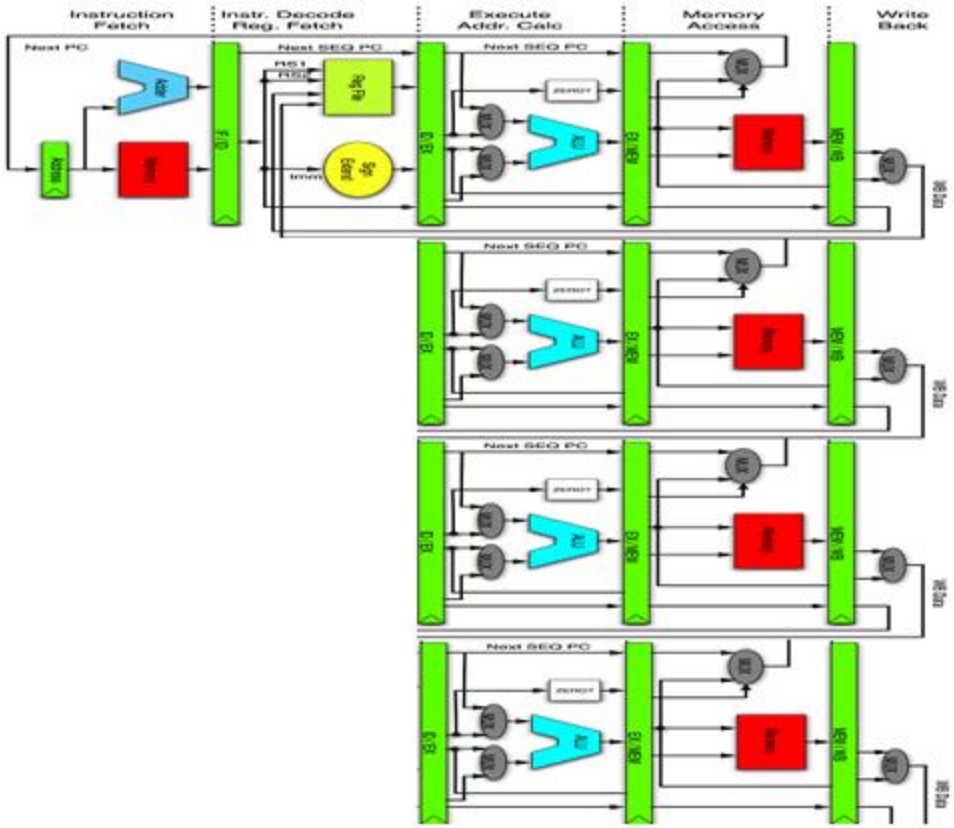

Implementation:

- Instruction fetch control logic shared
- Same instruction stream executed on
- Multiple pipelines
- Multiple different operands in parallel

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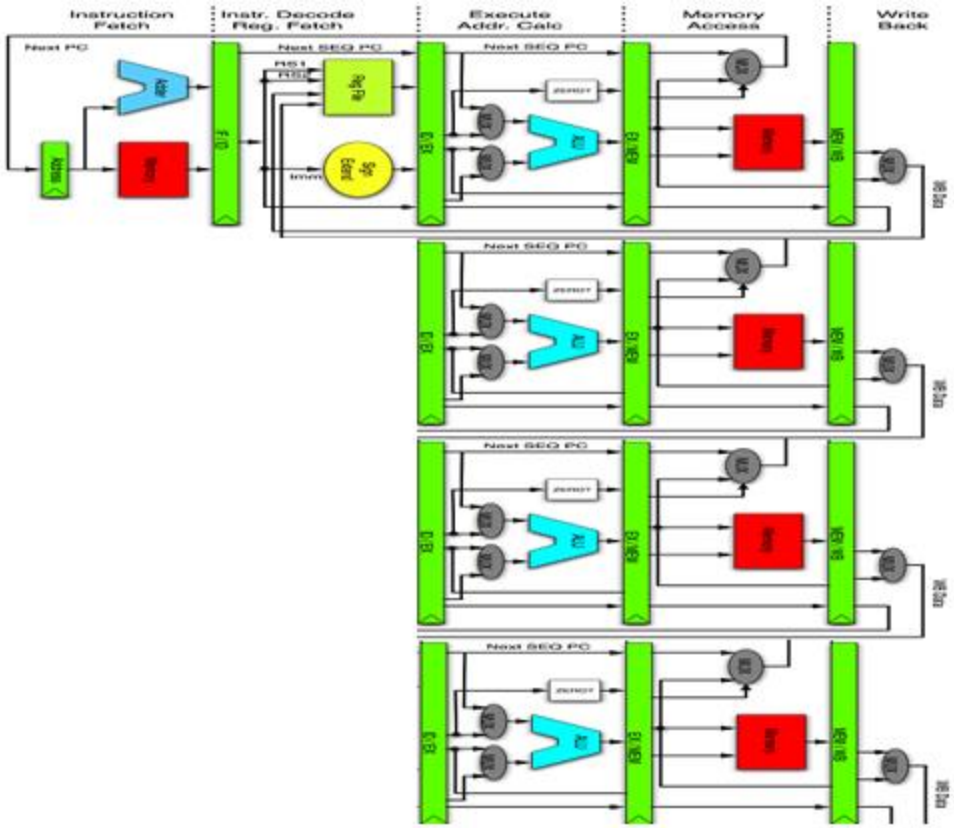

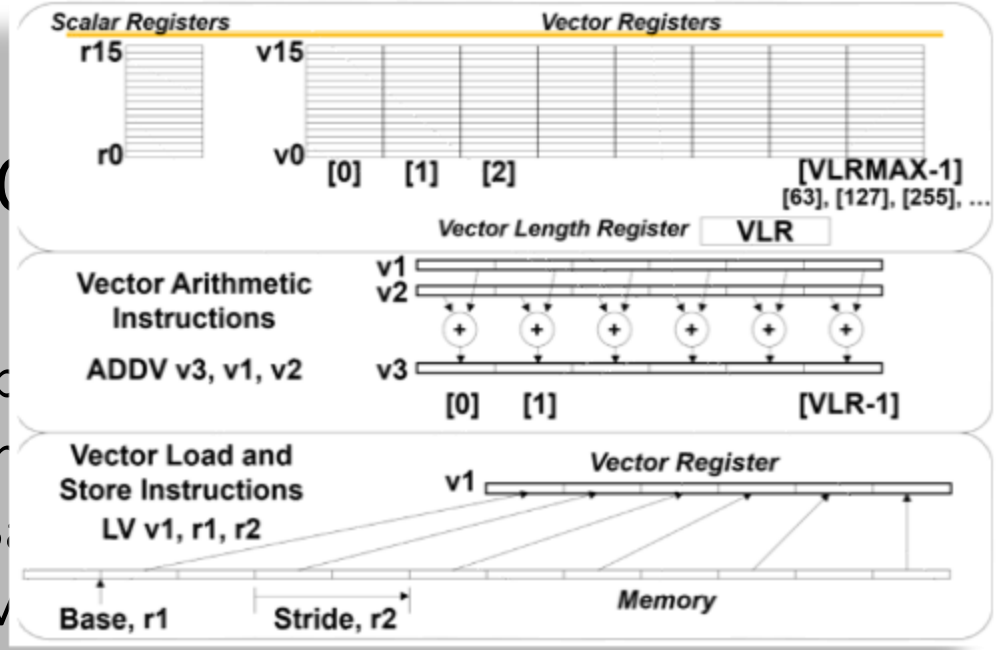

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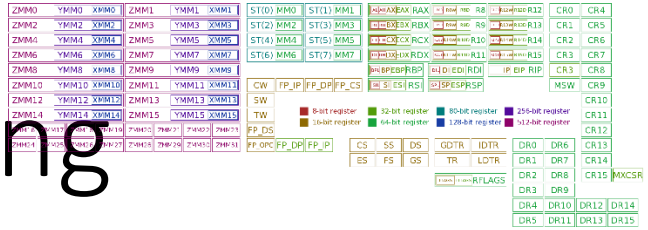

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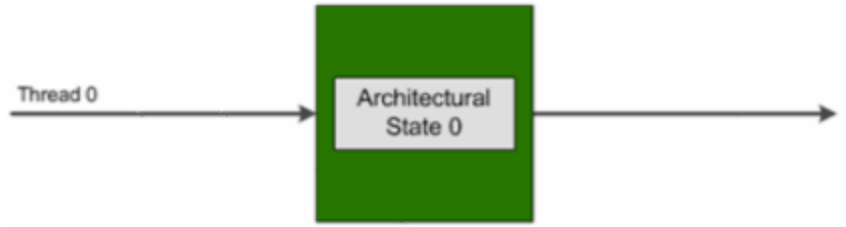

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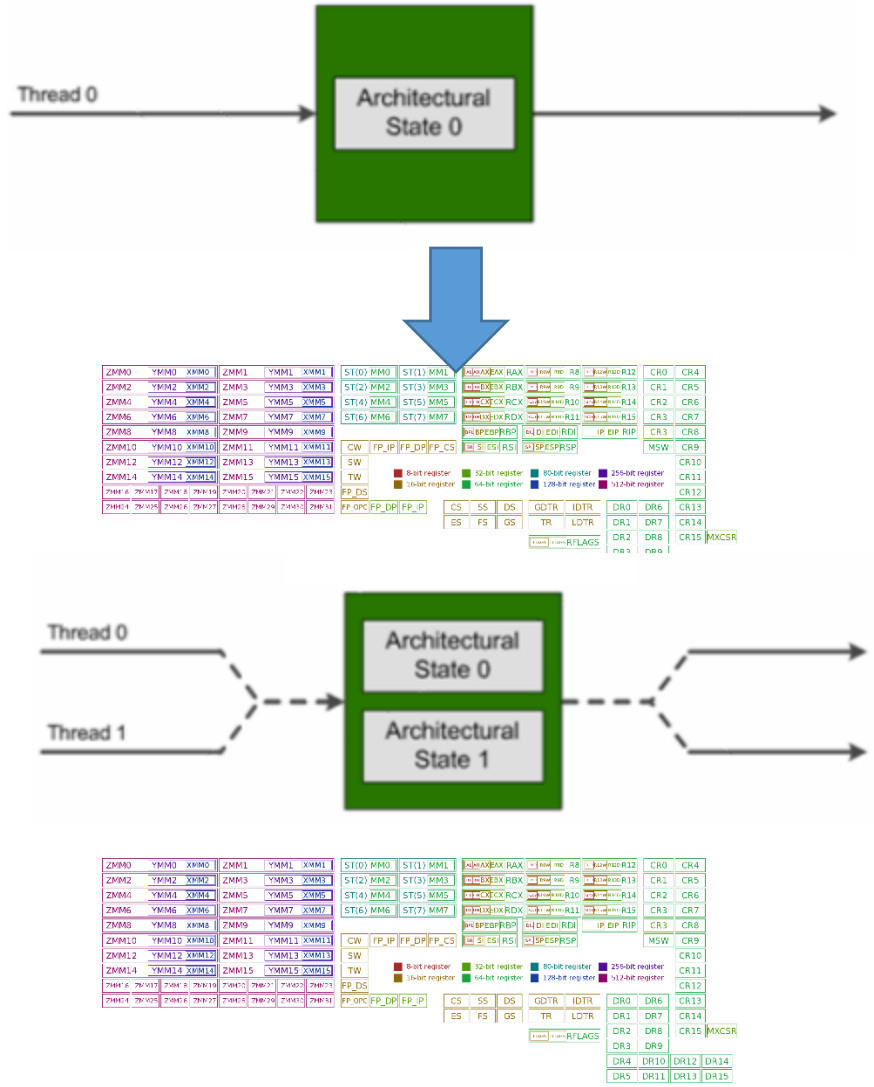

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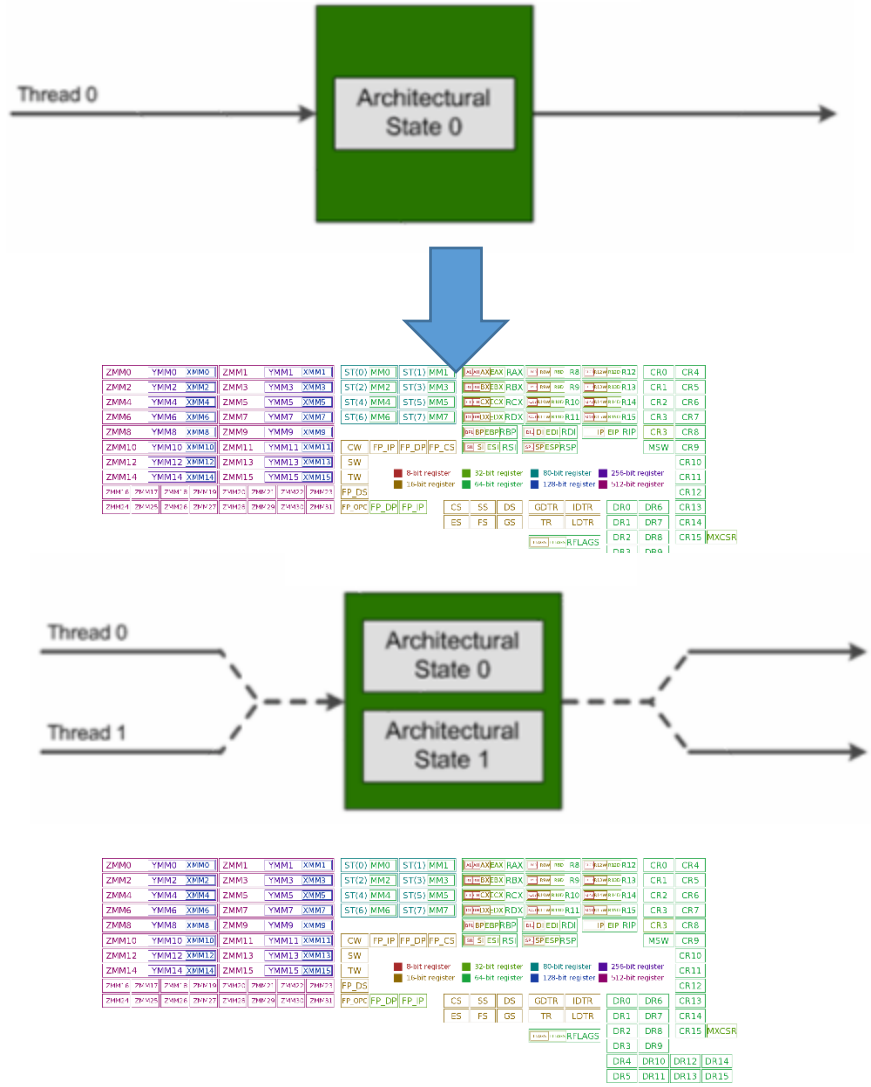

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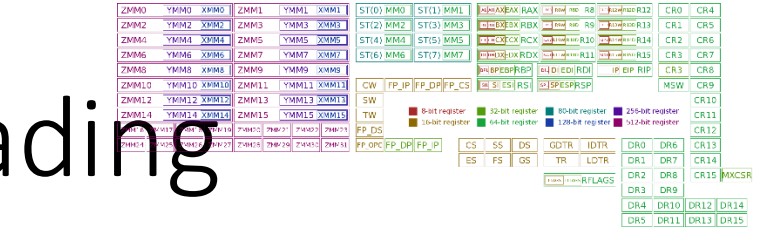
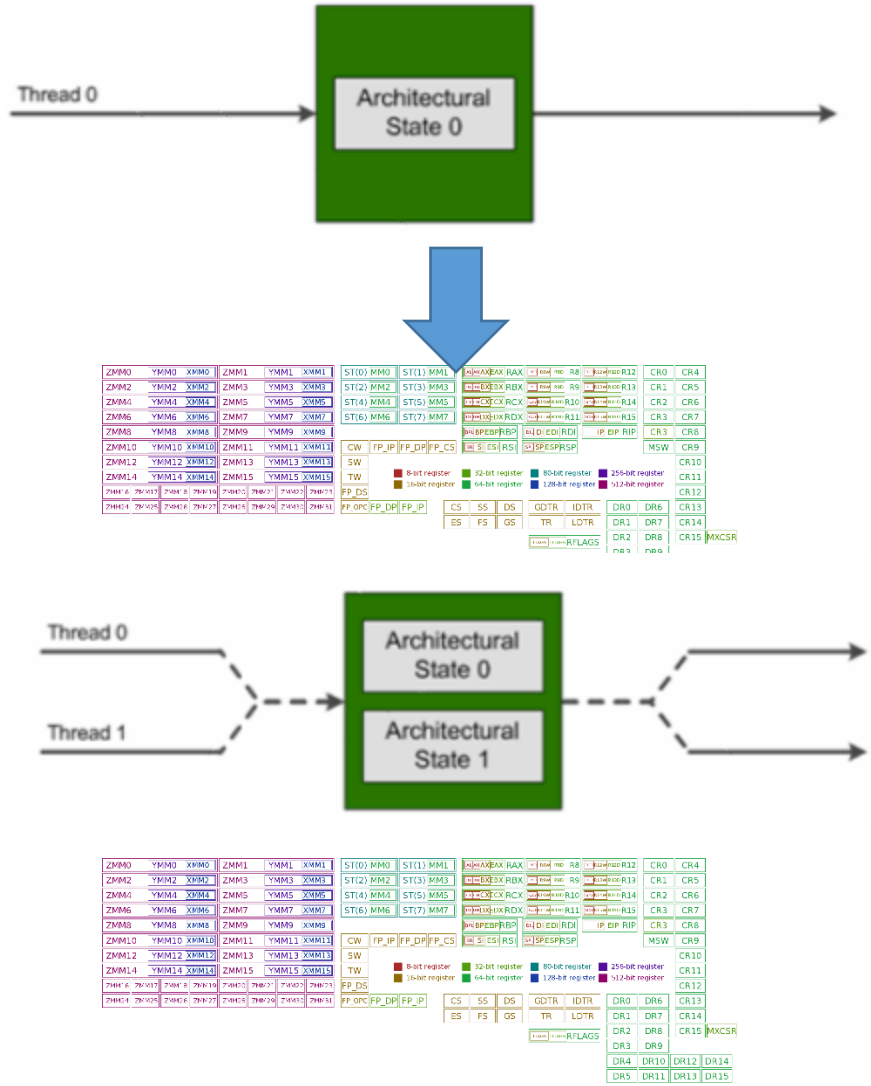
- Three variants:
  - Coarse
  - Fine-grain
  - Simultaneous





Programming Model

- ***GPUs are I/O devices, managed by user-code***
- “kernels” == “shader programs”
- 1000s of HW-scheduled threads per kernel
- Threads grouped into independent blocks.
  - Threads in a block can synchronize (barrier)
  - This is the *only* synchronization
- “Grid” == “launch” == “invocation” of a kernel
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Need codes that are 1000s-X parallel….

Parallel Algorithms

- Sequential algorithms often do not permit easy parallelization
  - Does not mean there work has no parallelism
  - A different approach can yield parallelism
  - but often changes the algorithm
  - Parallelizing != just adding locks to a sequential algorithm
- Parallel Patterns
  - Map
  - Scatter, Gather
  - Reduction
  - Scan
  - Search, Sort

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If you can express your algorithm using these patterns, an apparently fundamentally sequential algorithm can be made parallel

Map

- Inputs
  - Array A
  - Function f(x)
- map(A, f) → apply f(x) on all elements in A
- Parallelism trivially exposed
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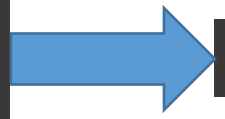
```
for(i=0; i<numPoints; i++) {
   labels[i] = findNearestCenter(points[i]);
}
```



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map(points, findNearestCenter)
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Scatter and Gather

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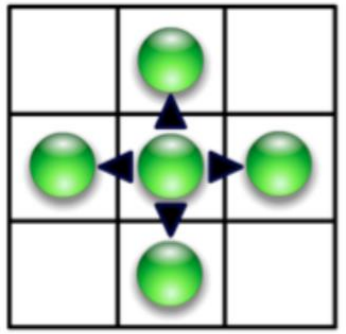
→ scatter(x, y, idx)



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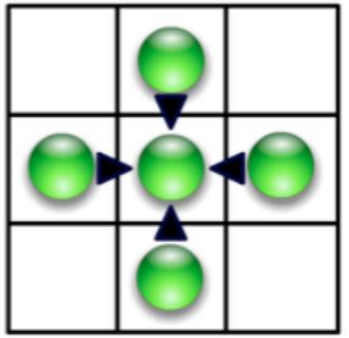

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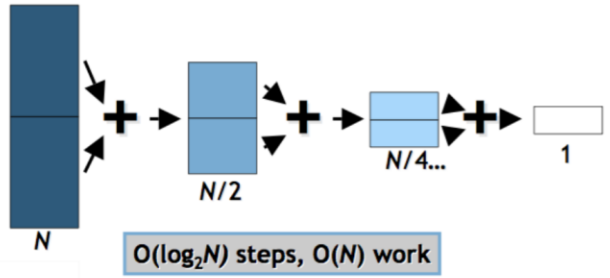

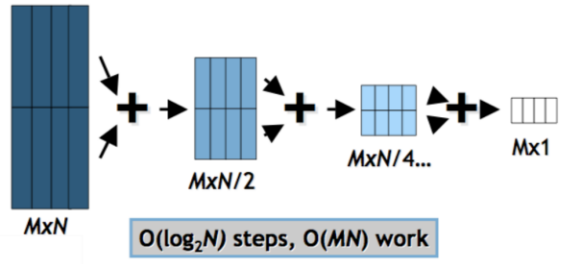


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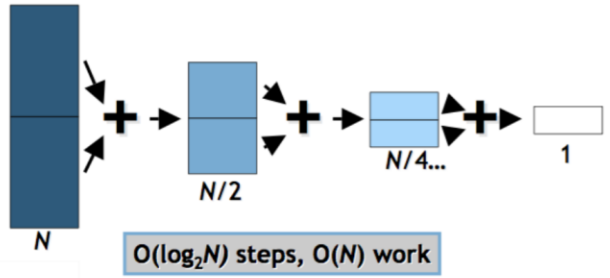

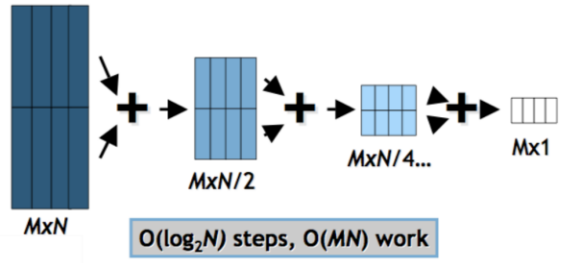


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Why must op be associative?

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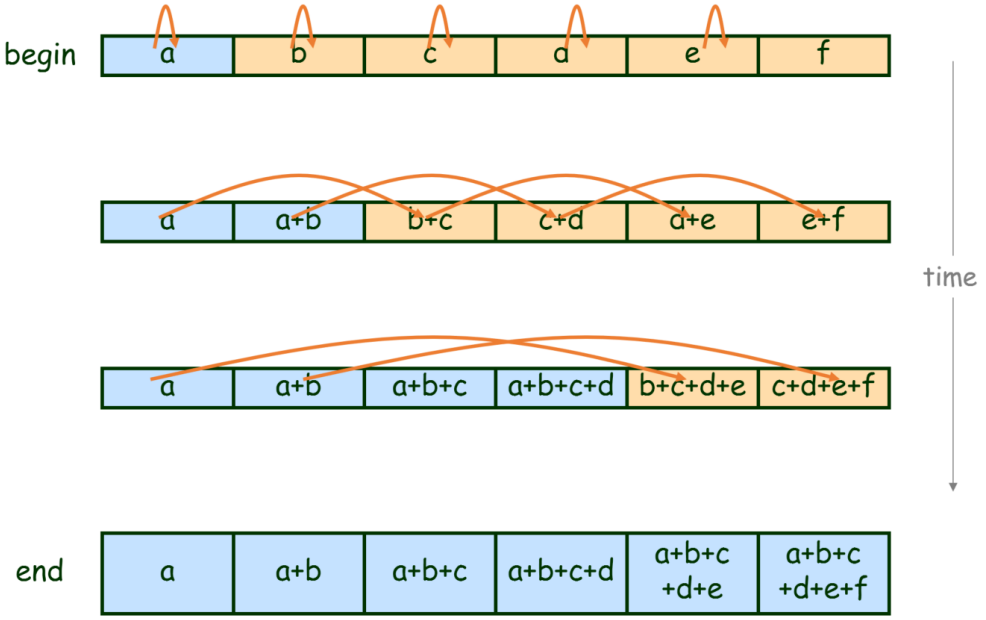

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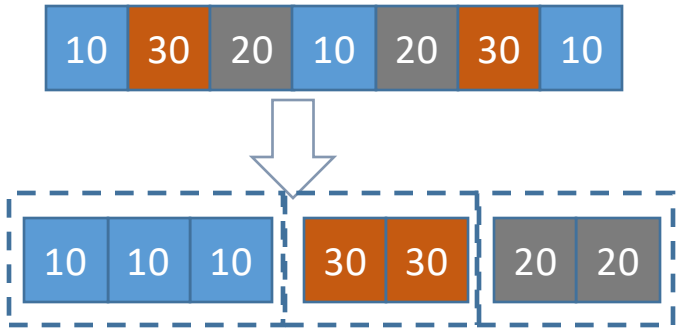

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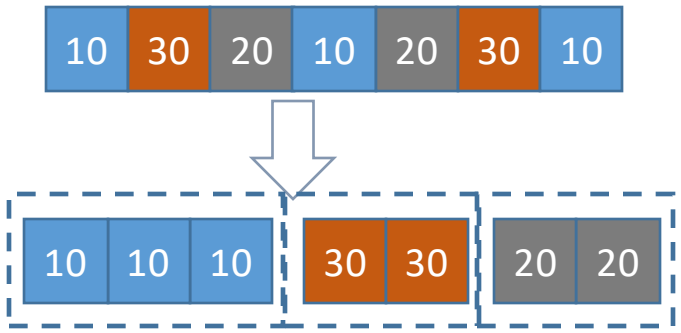


```
foreach(T elem in PF(ints))
{
  key   = KeyLambda(elem);

  group = GetGroup(key)

  group.Add(elem);
}
```

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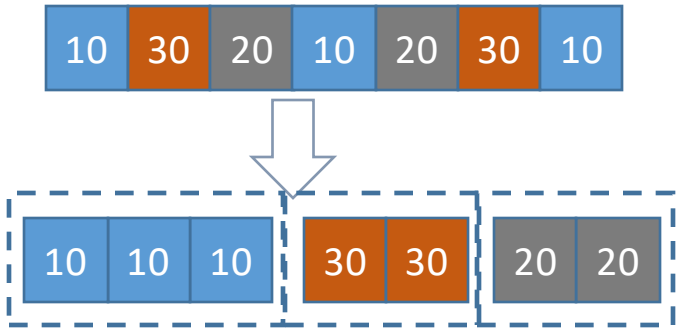
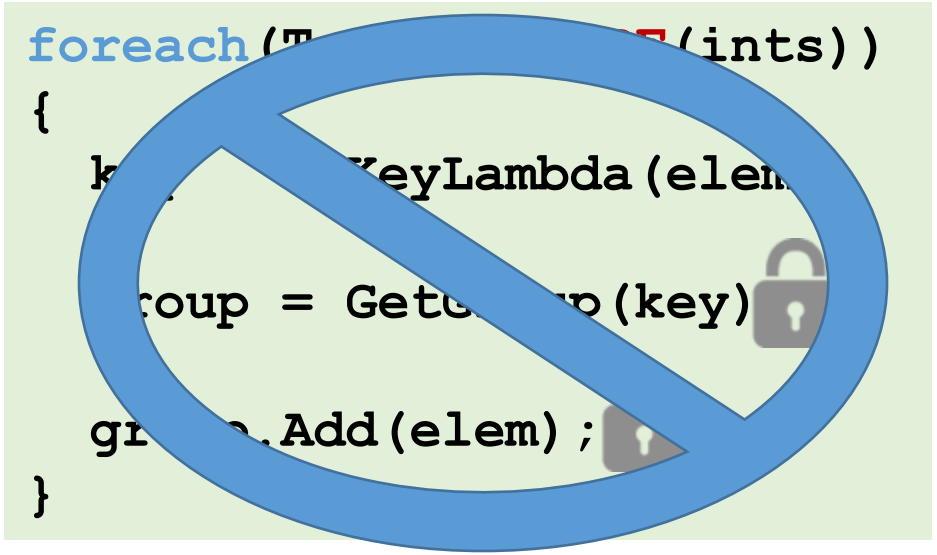
- *Insufficient Parallelism*
- *Requires synchronization*





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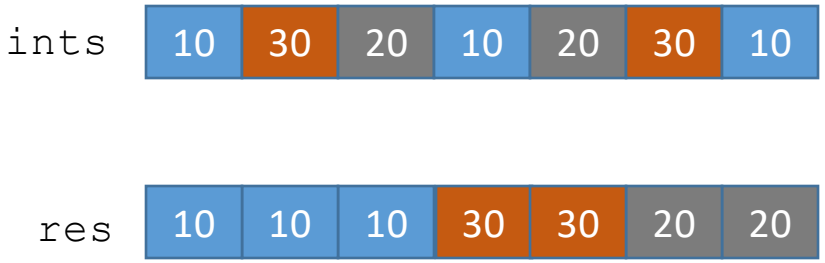
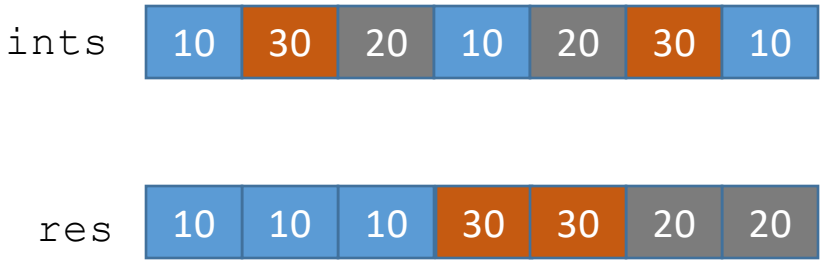


Parallel GroupBy

Process each input element in parallel

- grouping ~ shuffling
- input item → output offset such that groups are contiguous



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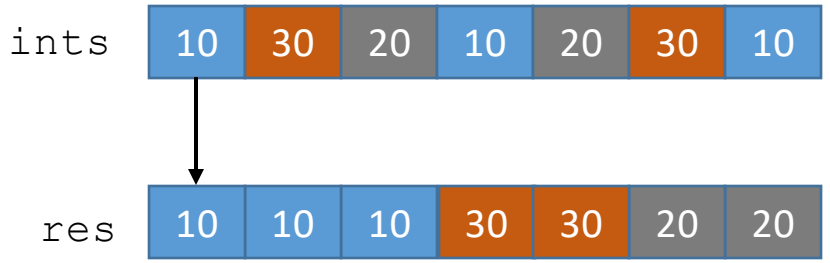

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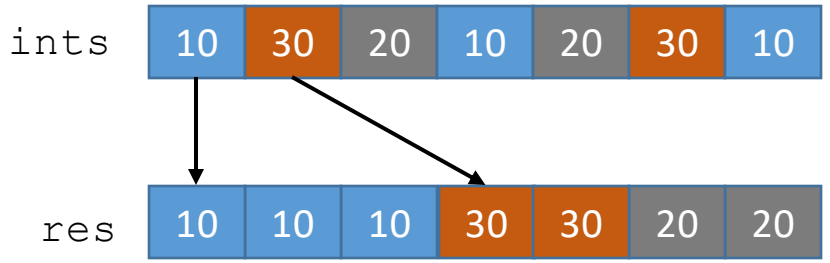

Parallel GroupBy

Process each input element in parallel

- grouping ~ shuffling
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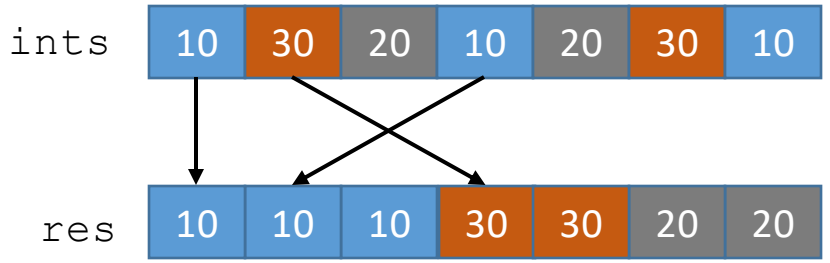

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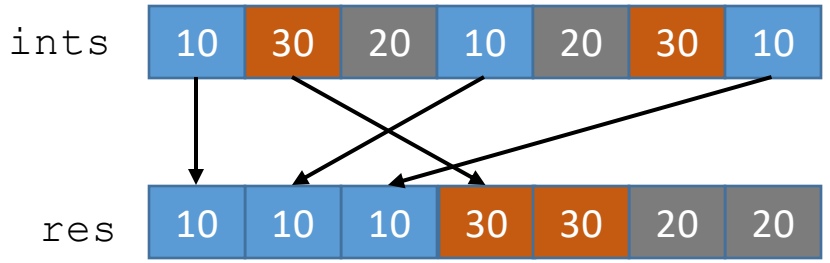

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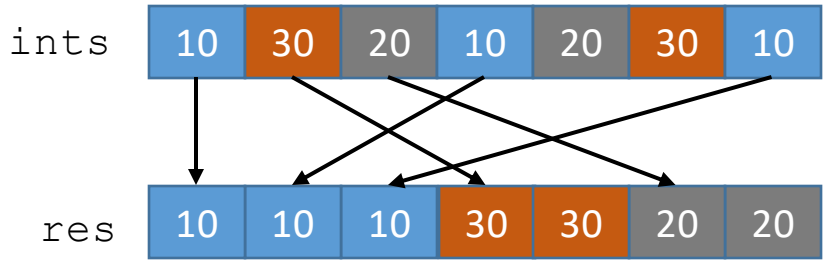

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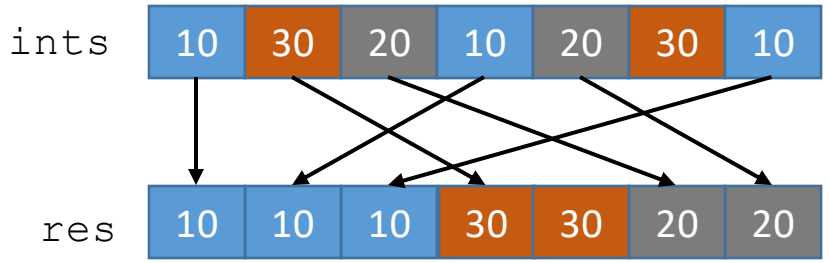

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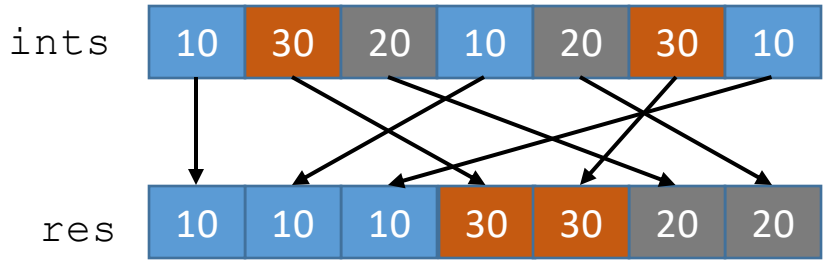

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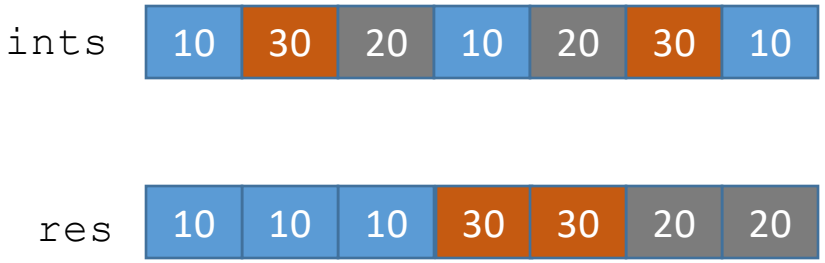

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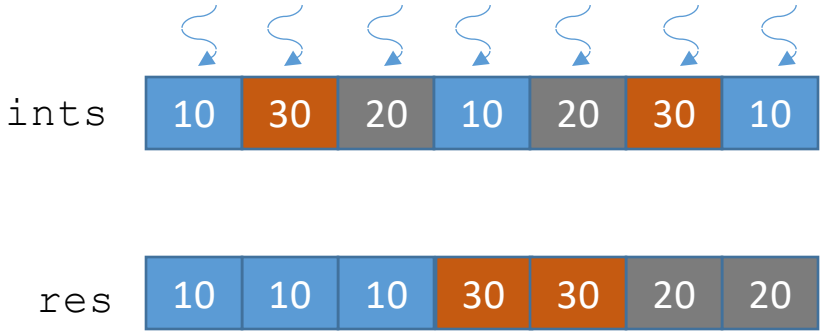

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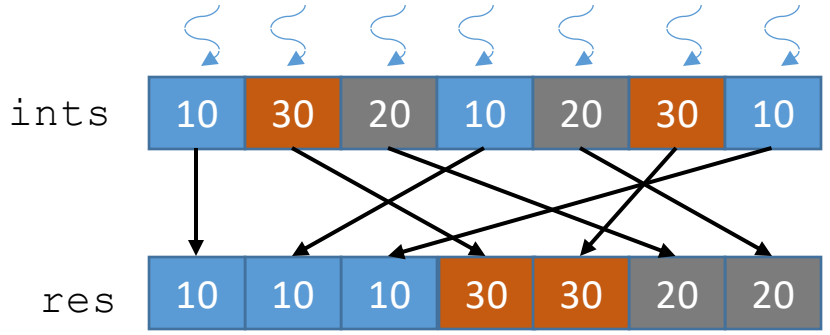

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Process each input element in parallel

- grouping ~ shuffling
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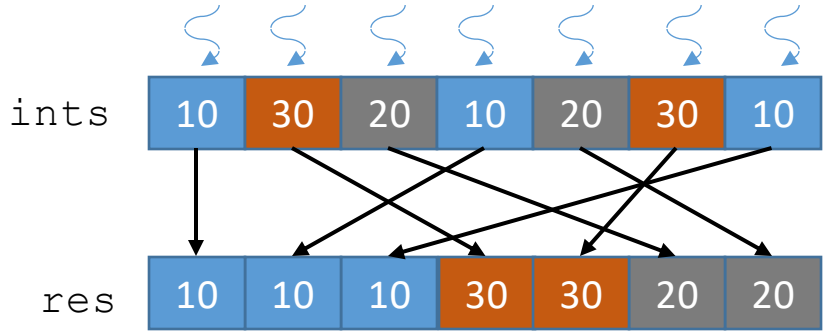
- output offset = group offset + item number
- … but how to get the group offset, item number?



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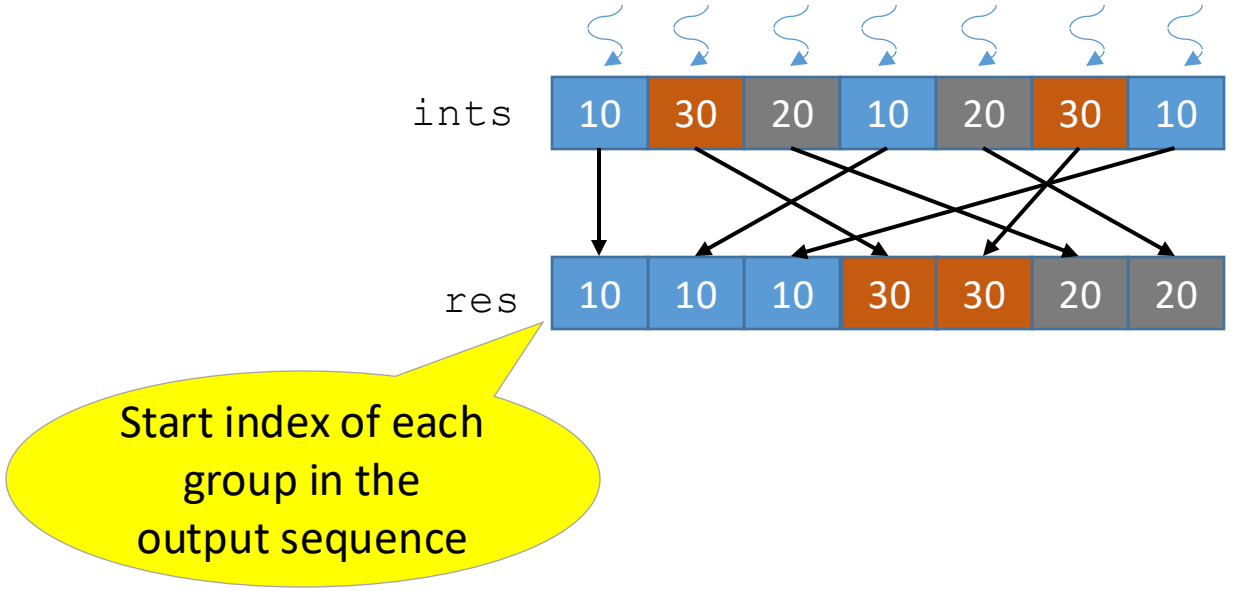

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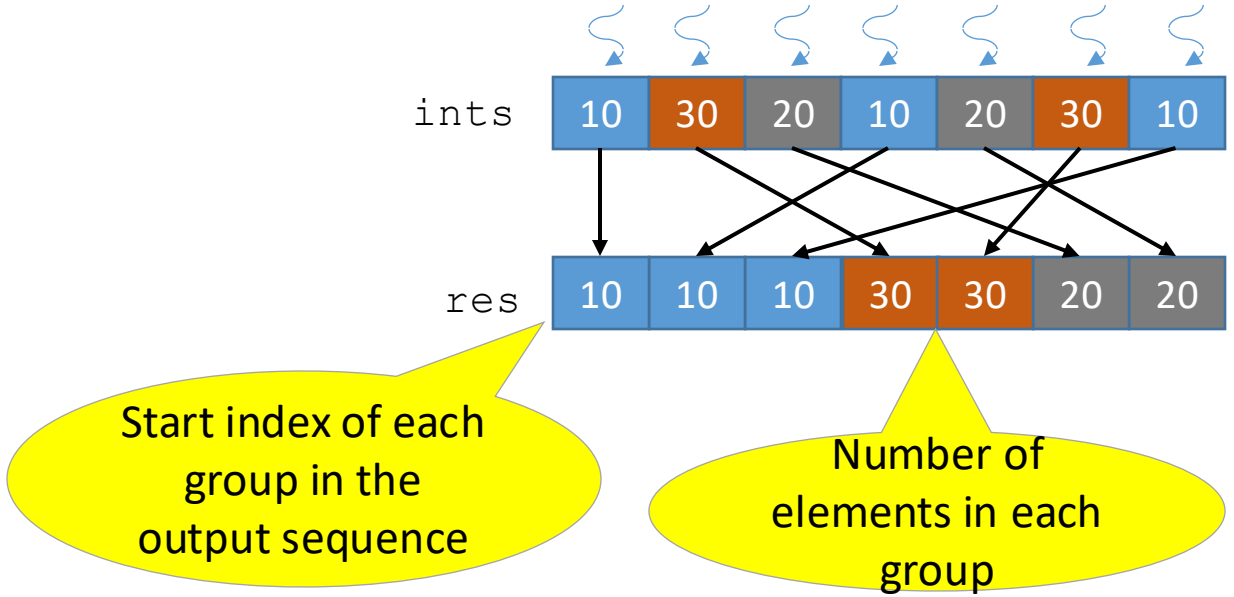

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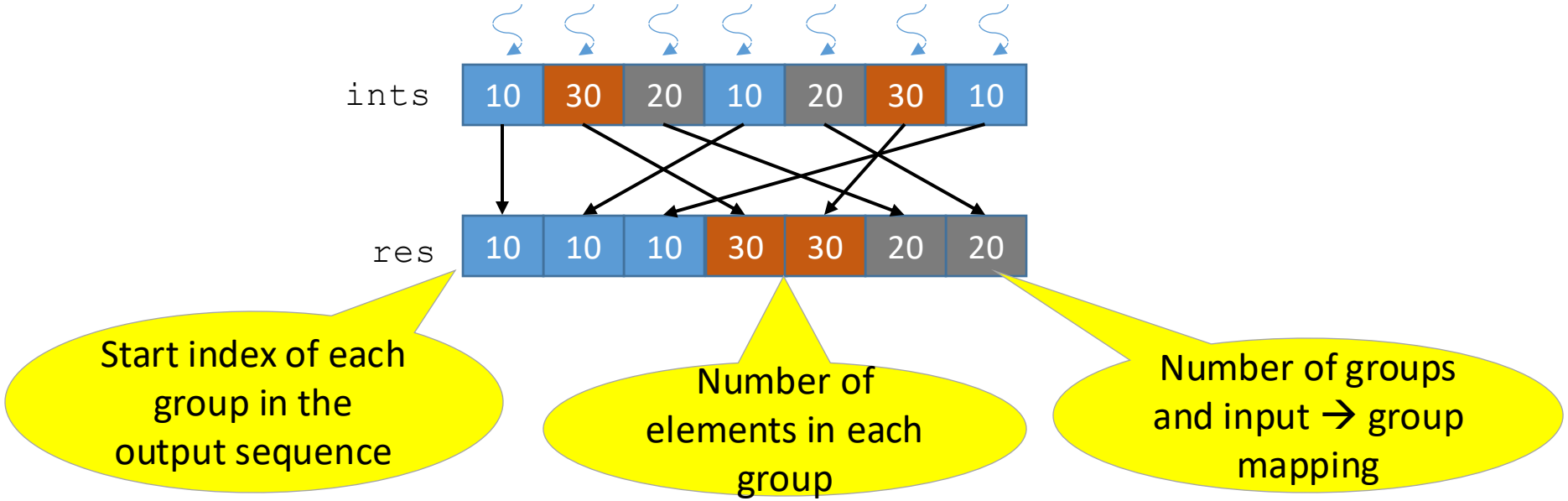

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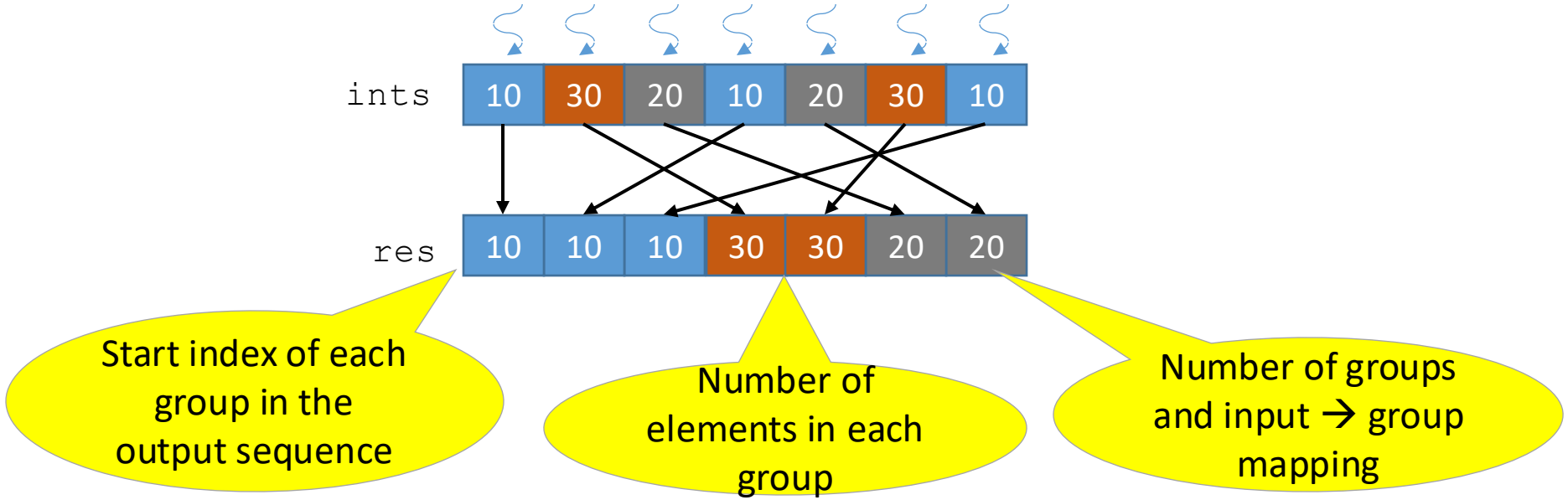

GroupBy using parallel primitives

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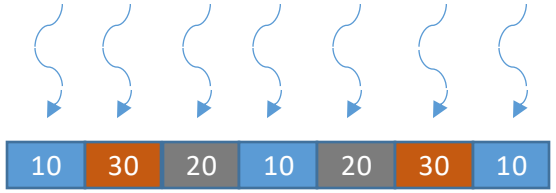

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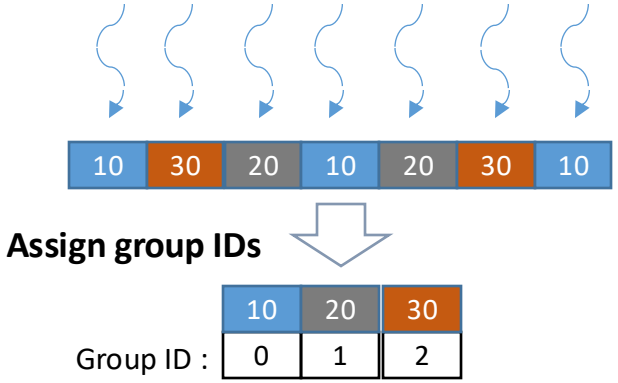

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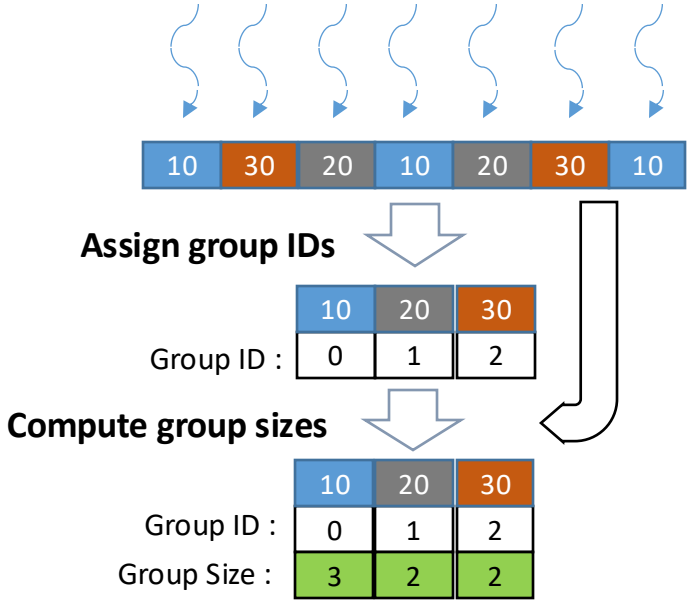

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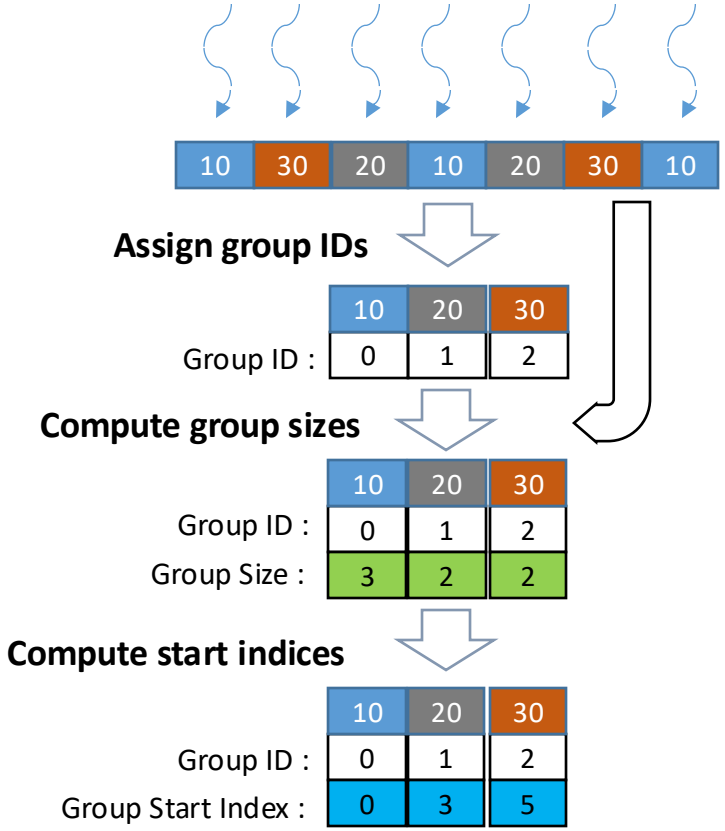

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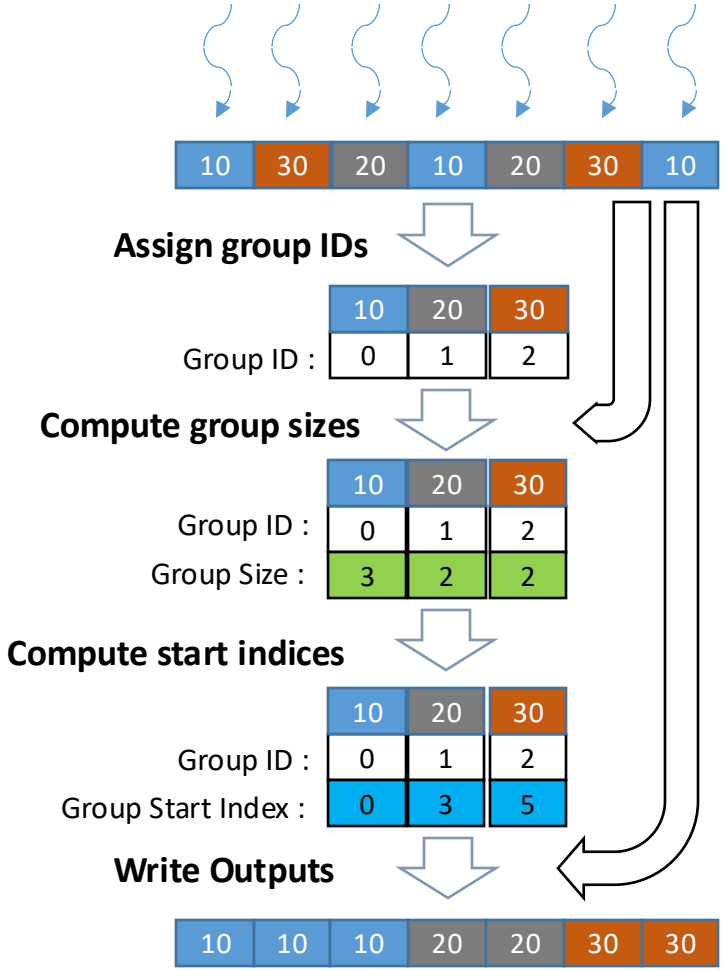

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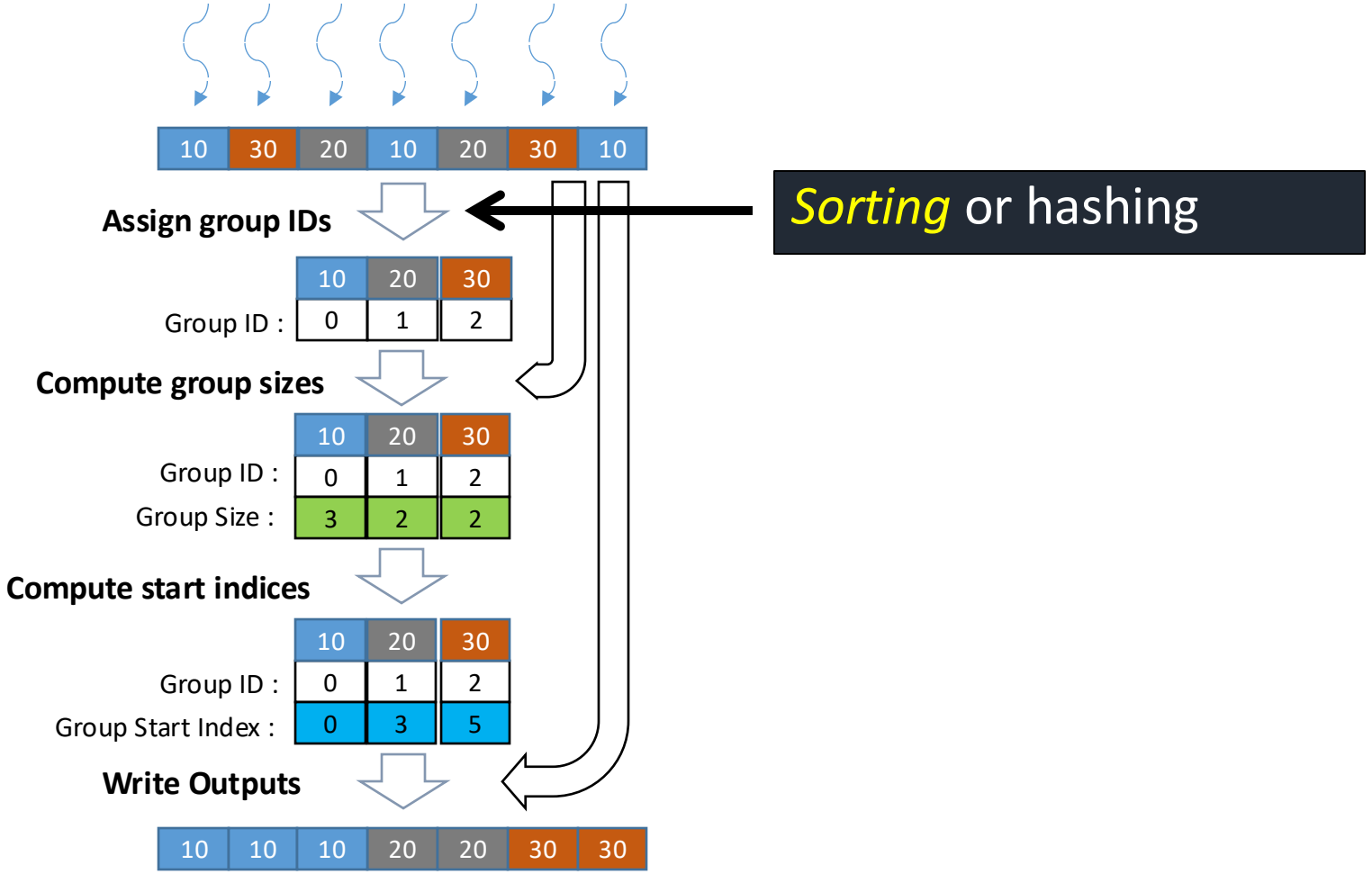

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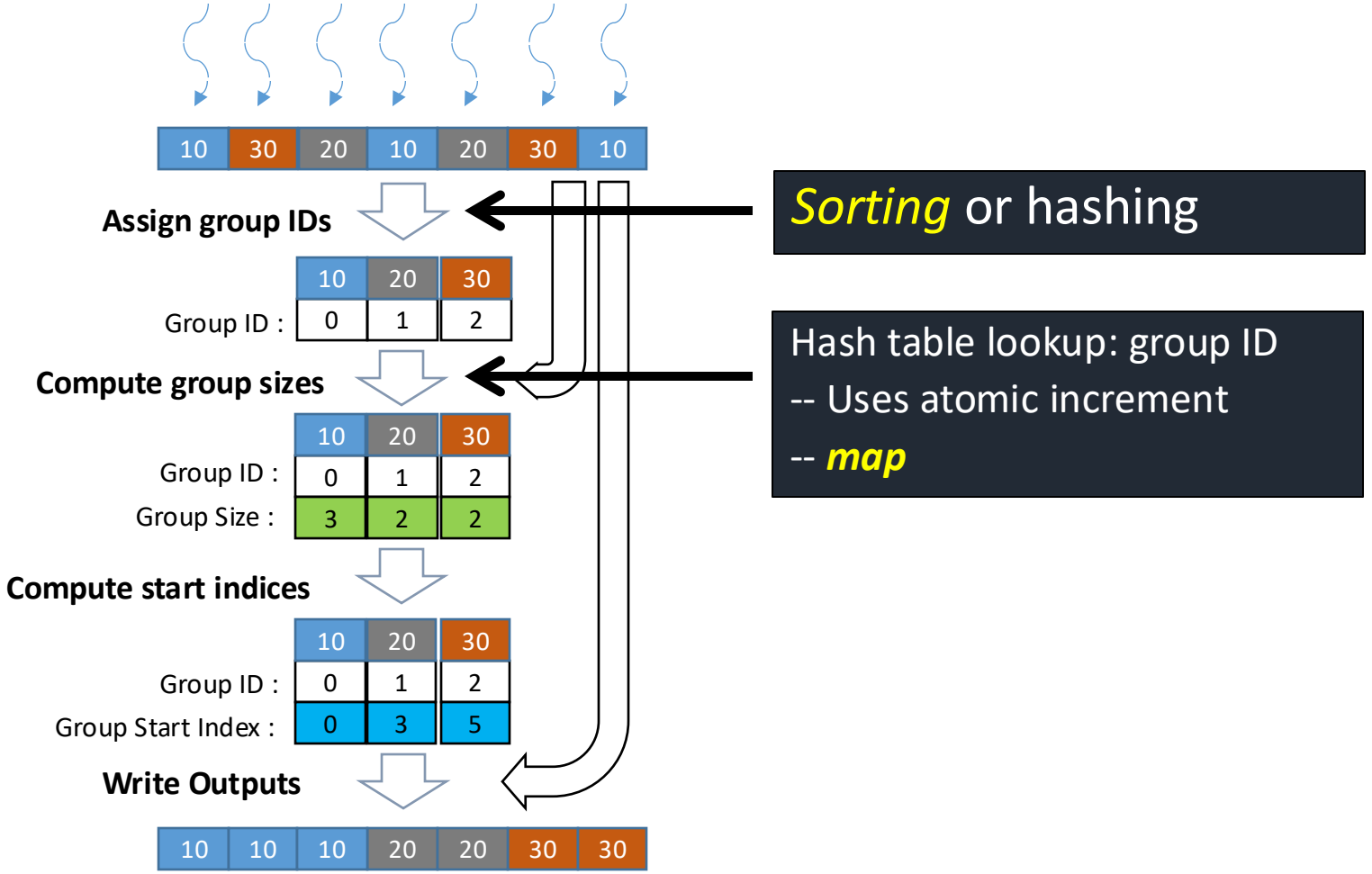

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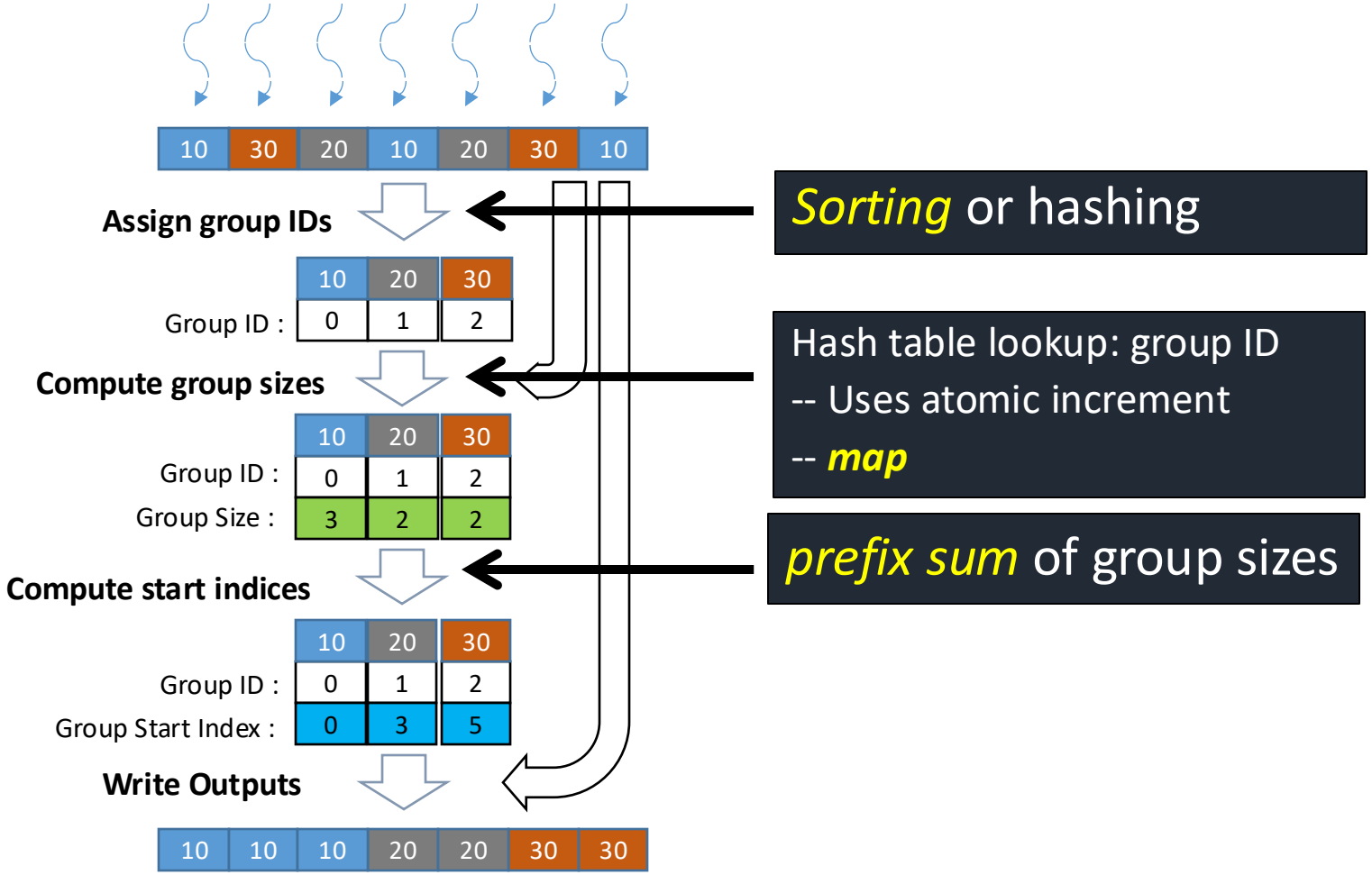

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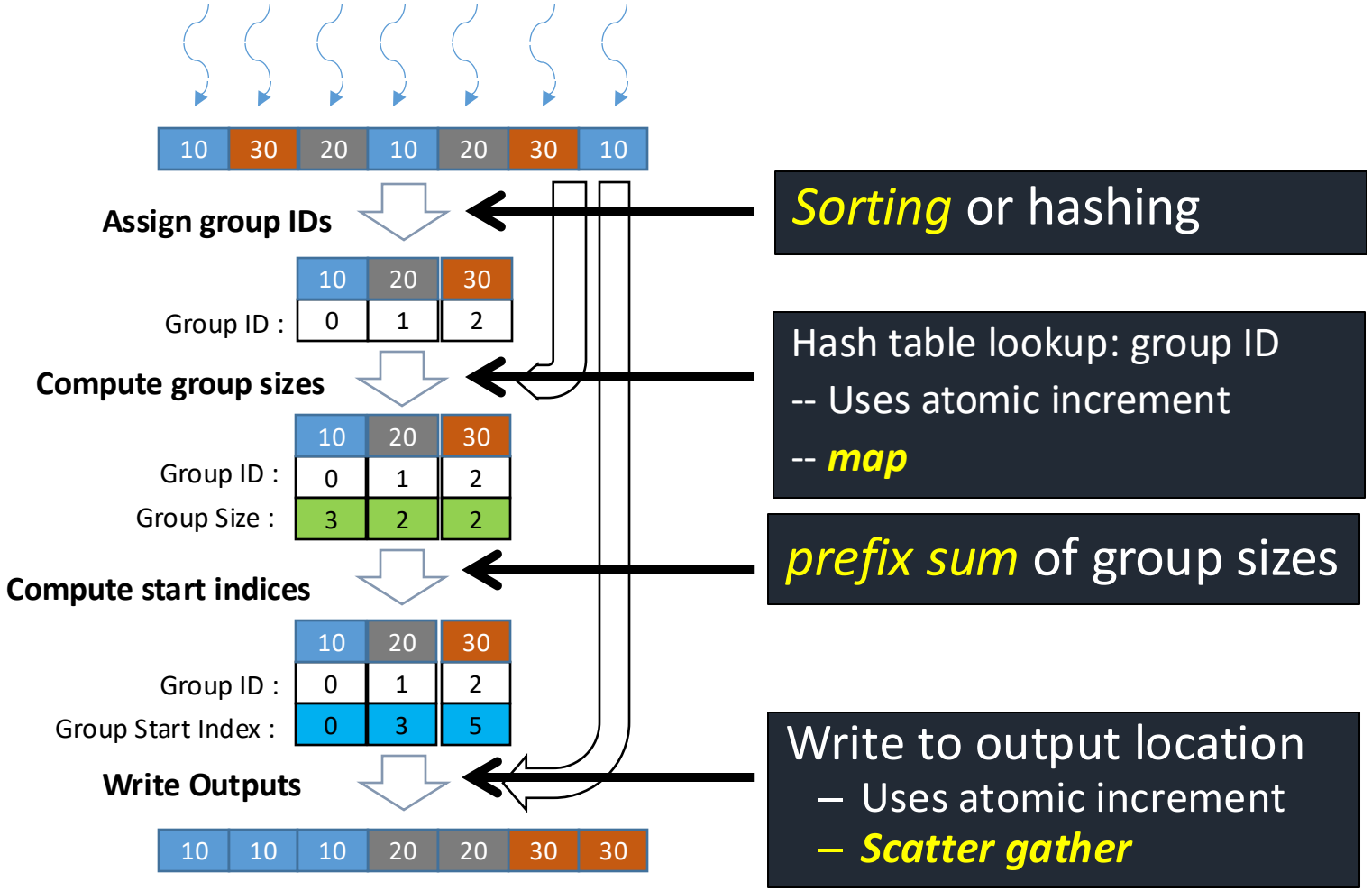

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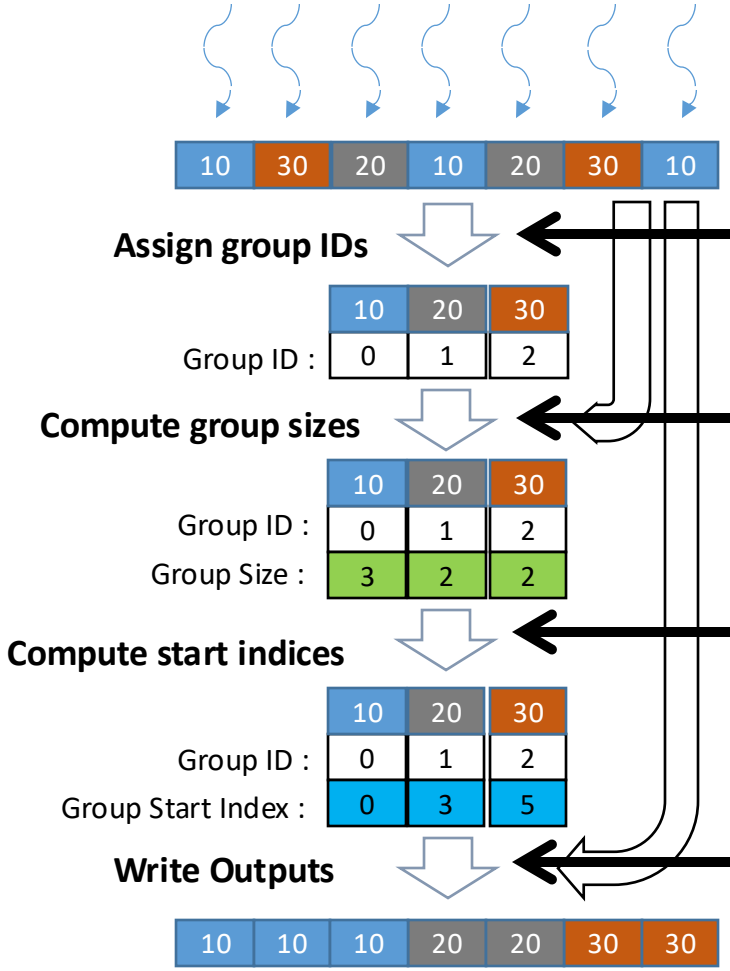

Sorting or hashing

Hash table lookup: group ID
-- Uses atomic increment
-- ***map***

prefix sum of group sizes

Write to output location
– Uses atomic increment
– ***Scatter gather***

We'll revisit after more CUDA background…

Sort

Many variations

- Enumeration sort
- Bitonic sort
- Merge sort
- Parallel Quicksort
- Radix sort
- Sample sort
- …

Summary

Re-expressing apparently sequential algorithms as combinations of parallel patterns is a common technique when targeting GPUs

- Reductions
- Scans
- Re-orderings (scatter/gather)
- Sort
- Map