CS395T: Technology Driven Computer Architecture

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Today's Class

- Administrivia
- Student information sheets
- Course overview
  - Brief history of computer architecture
  - Technology and the microprocessor
  - Technology Trends

Pre-1958

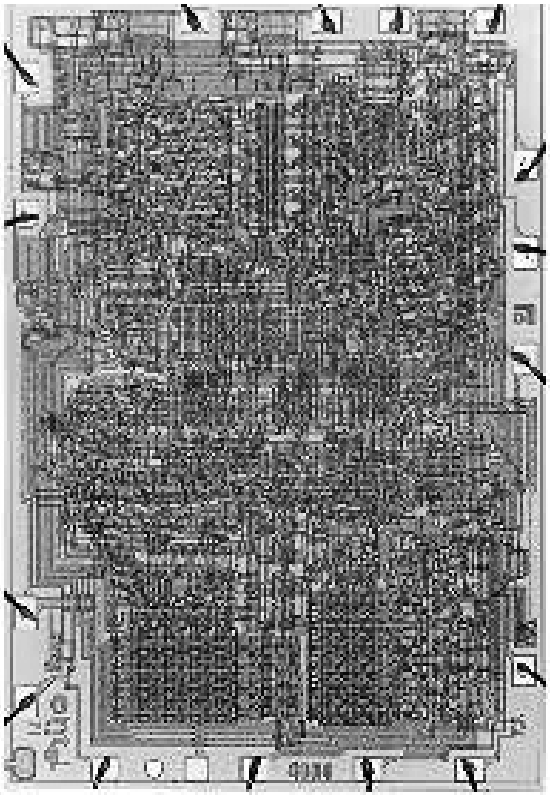
- 1948: Pennsylvania: ENIAC
  - 18,000 vacuum tubes, 200μs add
- 1949: Cambridge: EDSAC
  - First stored program computer, 1000μs add
- 1949: MIT: Whirlwind
  - Magnetic core memory, 8μs add
- 1955: IBM 704
  - First commercial floating-point hardware

Era of the Transistor

- 1962: Atlas (England)
  - Virtual memory
- 1964: Control Data 6600
  - Multiple arithmetic units, instruction re-ordering
- 1965: IBM 360
  - Introduction of the cache

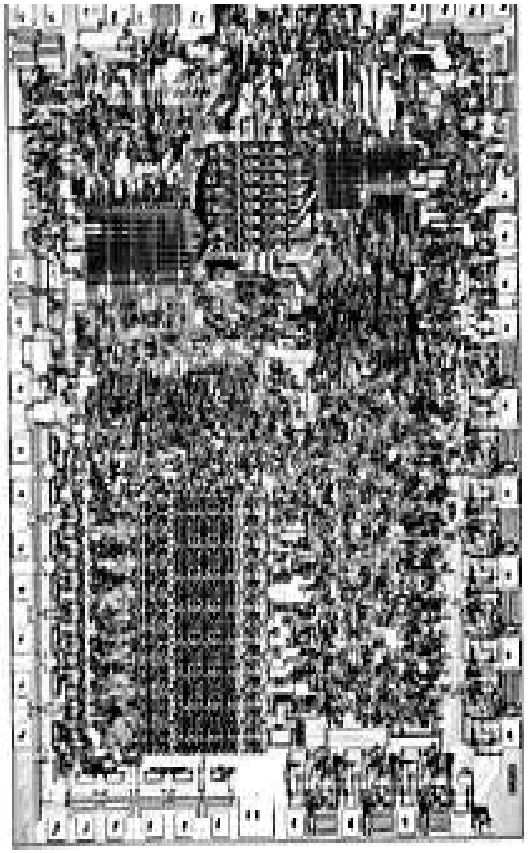
- 1967 - Integrated circuits take hold

1971: Intel 4004



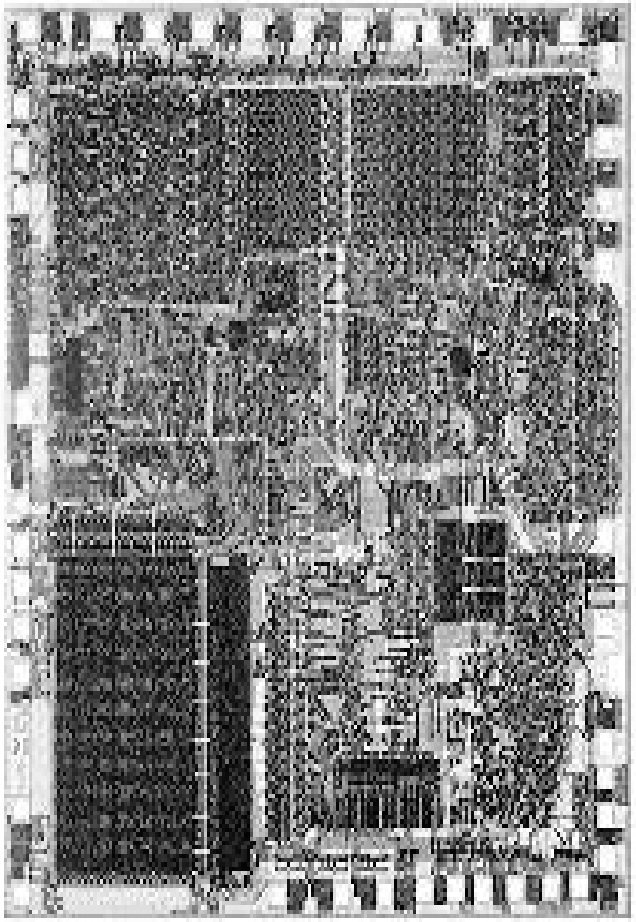
- First microprocessor
- 10 micron process
- 2,300 transistors
- 4 bit bus
- 640 bytes addressable memory
- 750KHz

1974: Intel 8080



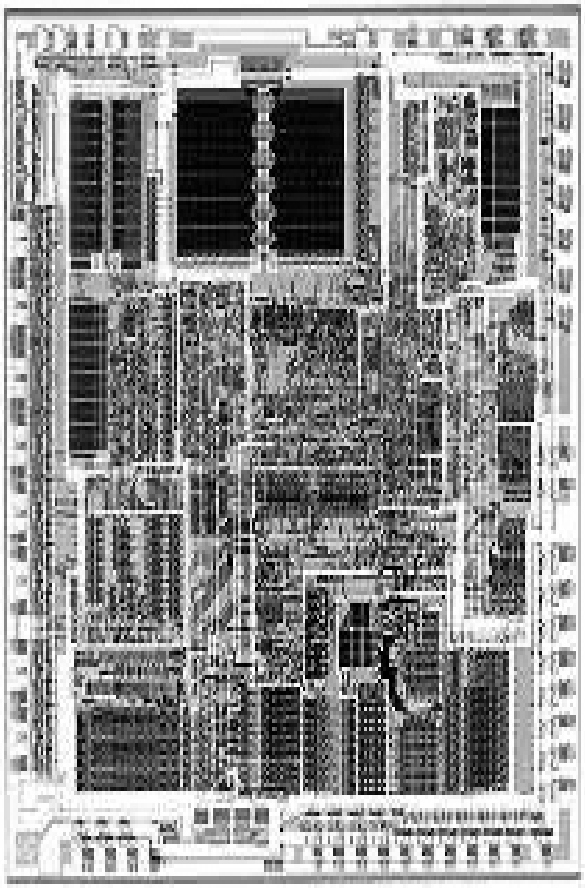
- Brain of first PC: Altair
- 6 micron process
- 6,000 transistors
- 8 bit bus
- 64KBytes addressable memory
- 2MHz

1978: Intel 8086



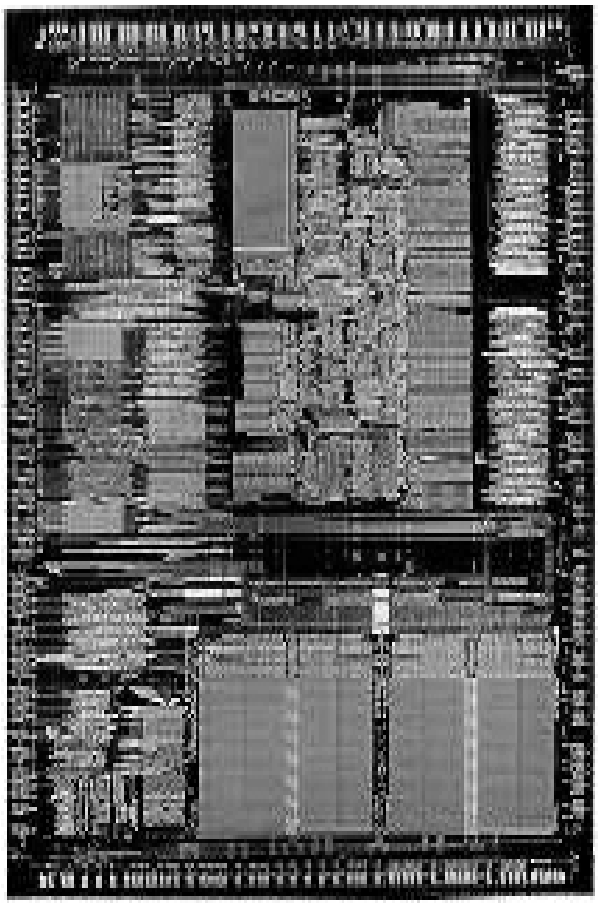
- First IBM PC chip
- 3 micron process
- 29,000 transistors
- 16 bit bus
- 1MB addressable memory
- 10MHz

1982: Intel 80286



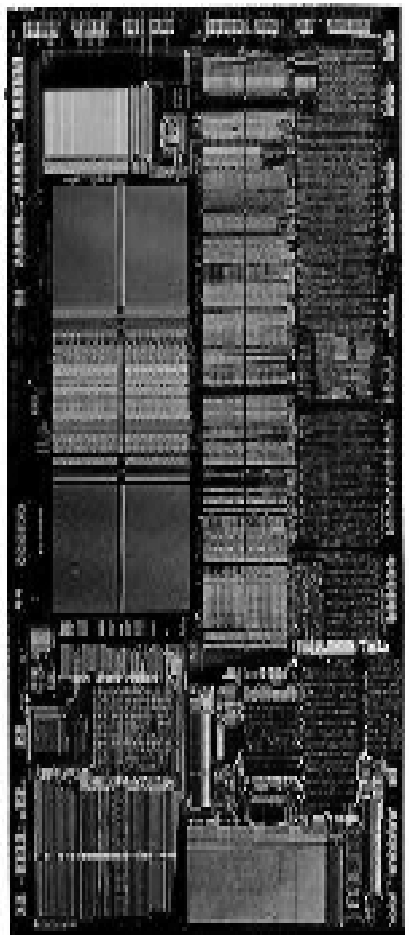
- Virtual memory
- 1.5 micron process
- 134,000 transistors
- 16 bit bus
- 16MB addressable memory
- 12.5MHz

1985: Intel 386



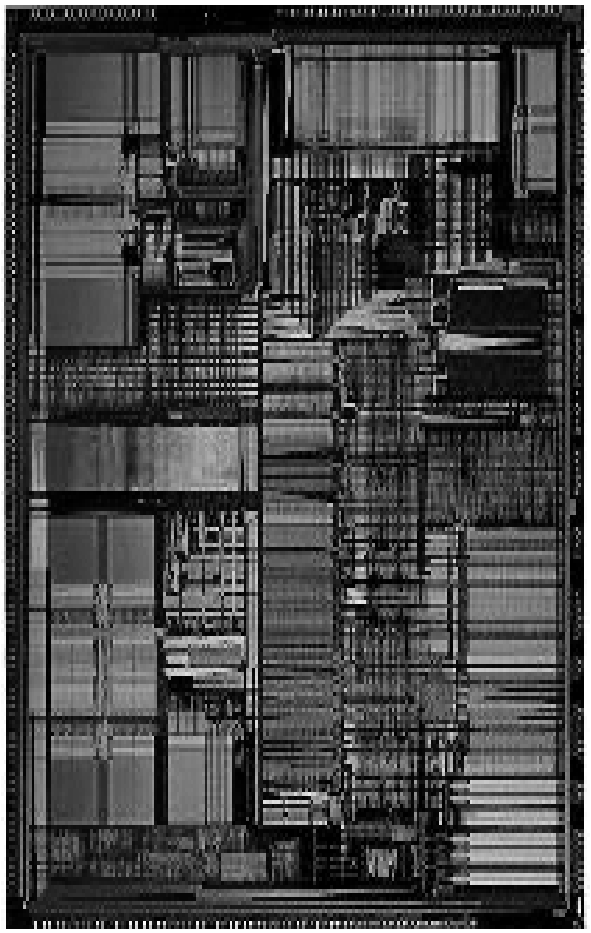
- On chip MMU
- 1 micron process
- 275,000 transistors
- 32 bit bus
- 4GB addressable memory
- 33MHz

1989: Intel 486



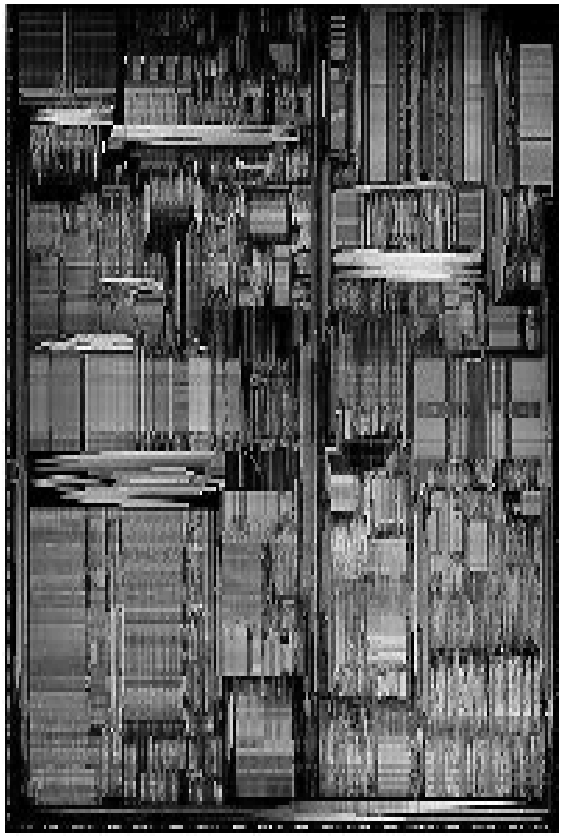
- On chip FPU, 8K cache, full pipelining
- 0.8 micron process
- 1.2 million transistors
- 32 bit bus
- 4GB addressable memory
- 50MHz

1993: Intel Pentium



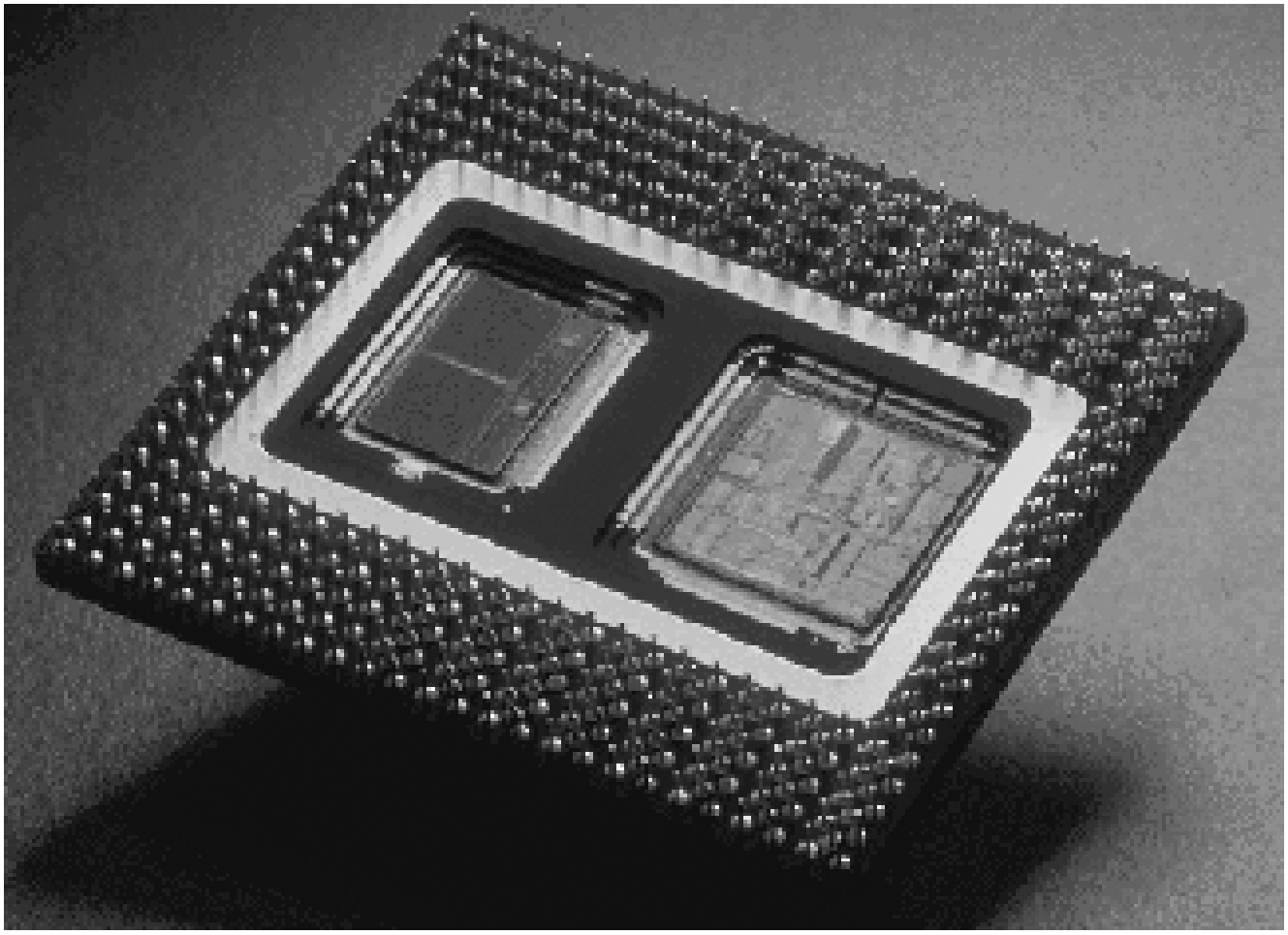
- 2-way superscalar, 8KB I/D caches
- 0.8 micron process
- 3.1 million transistors
- 32 bit bus
- 4GB addressable memory
- 166 MHz

1995: Pentium Pro

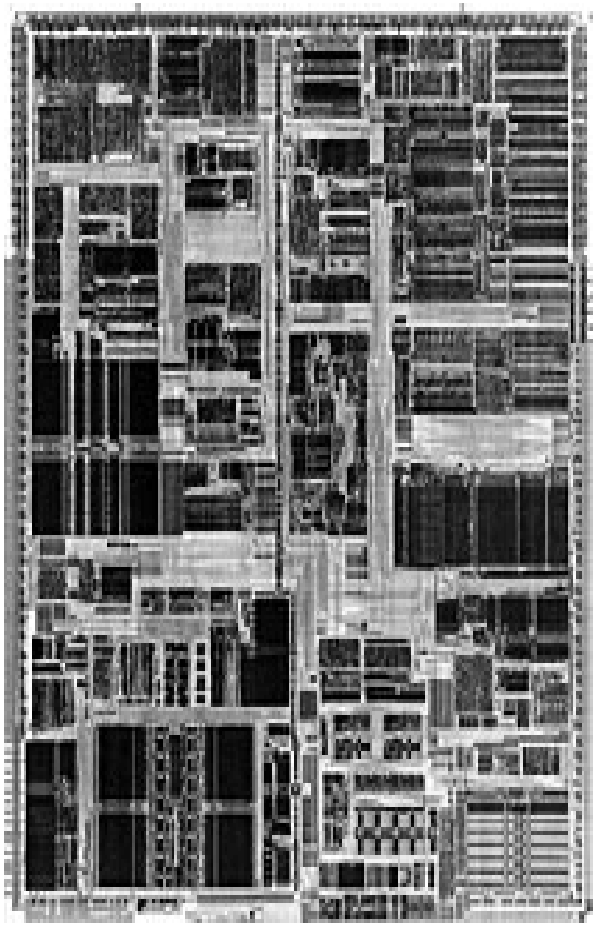


- Out-of-order, branch prediction, off-chip 512KB L2, 5 ALUs
- 0.6 micron process
- 5.5 million transistors
- 64 bit bus
- 64 TB addressable memory
- 200 MHz

Pentium Pro MCM

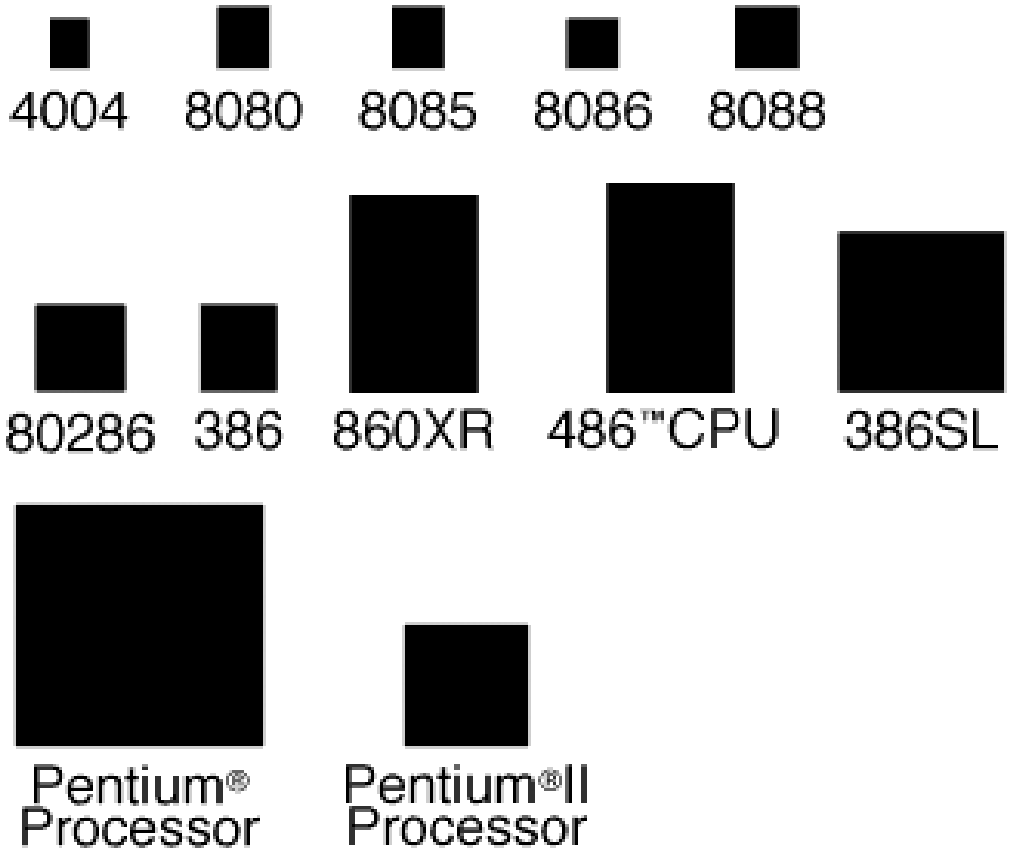


1997: Pentium II

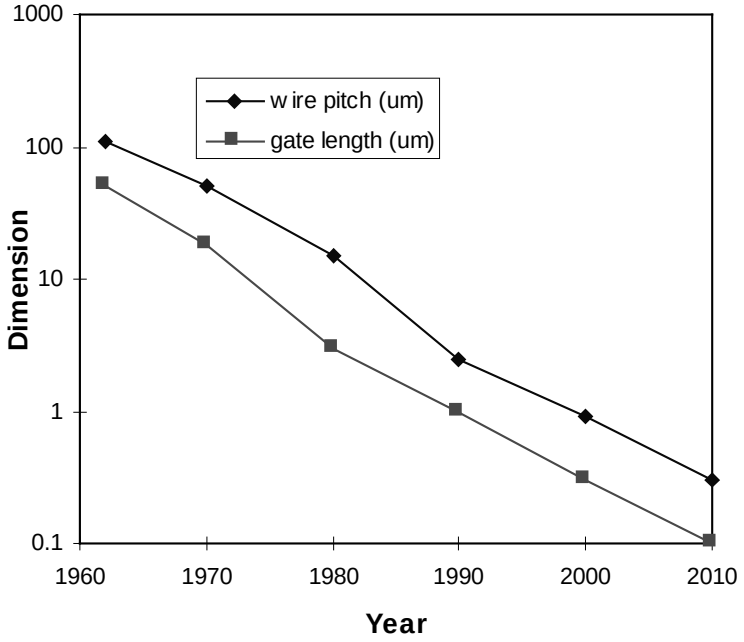


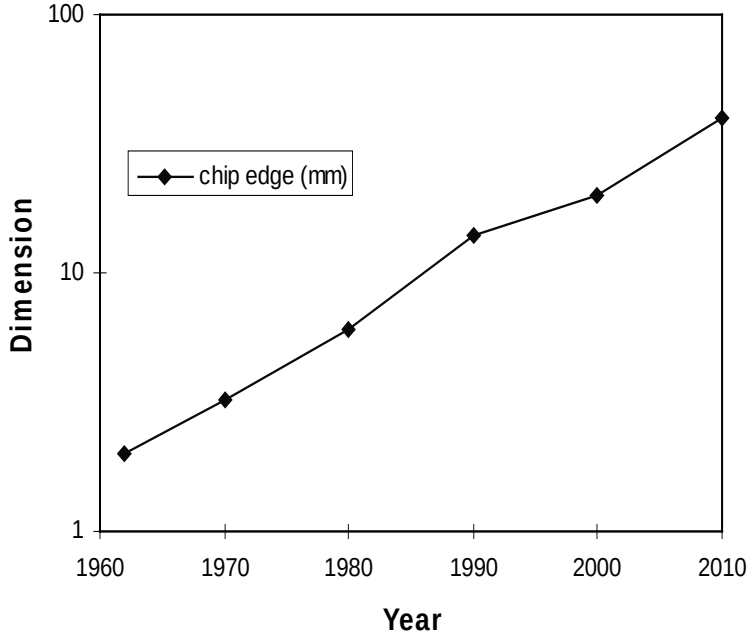
- 16 KB I/D caches, MMX
- 0.35 micron process
- 7.5 million transistors
- 64-bit bus
- 64 TB addressable memory
- 300MHz

Relative Sizes of Micros



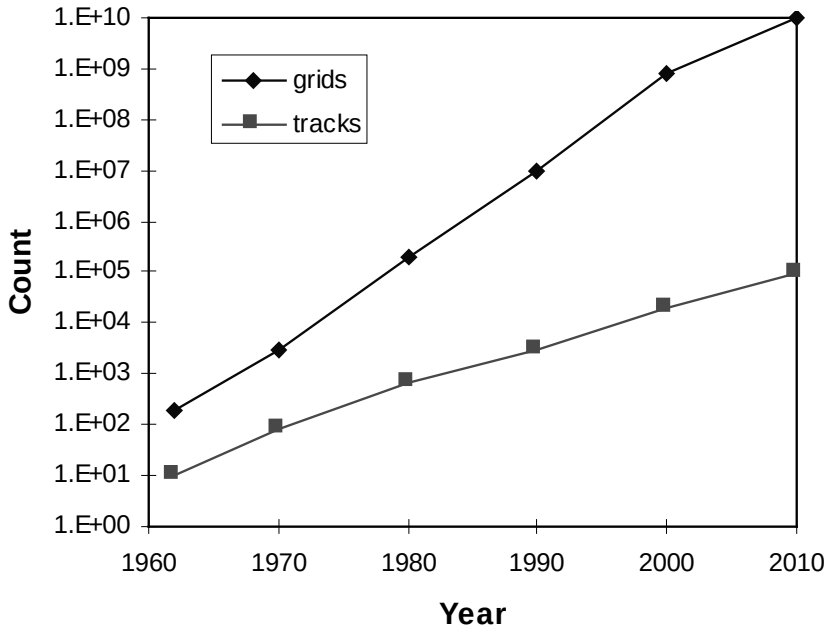
Chip Dimensions

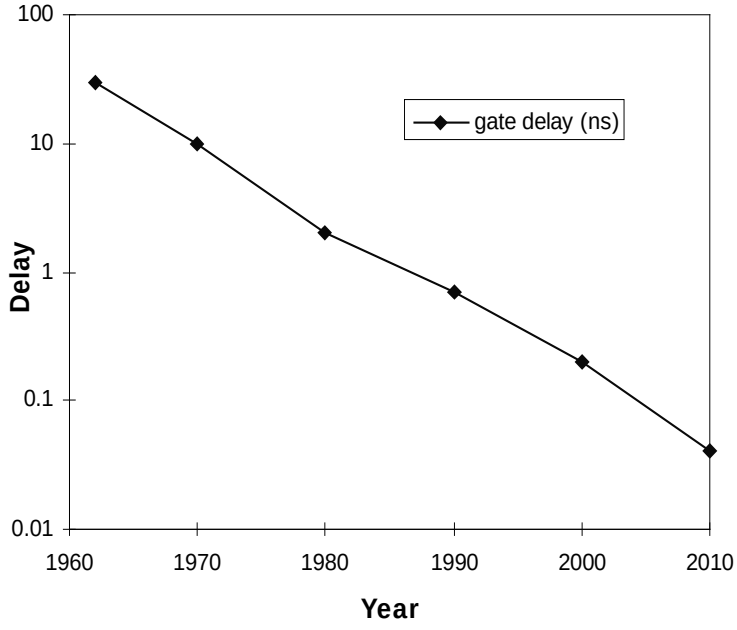




- **Feature size down 13%/year, Edge length up 6%/year**

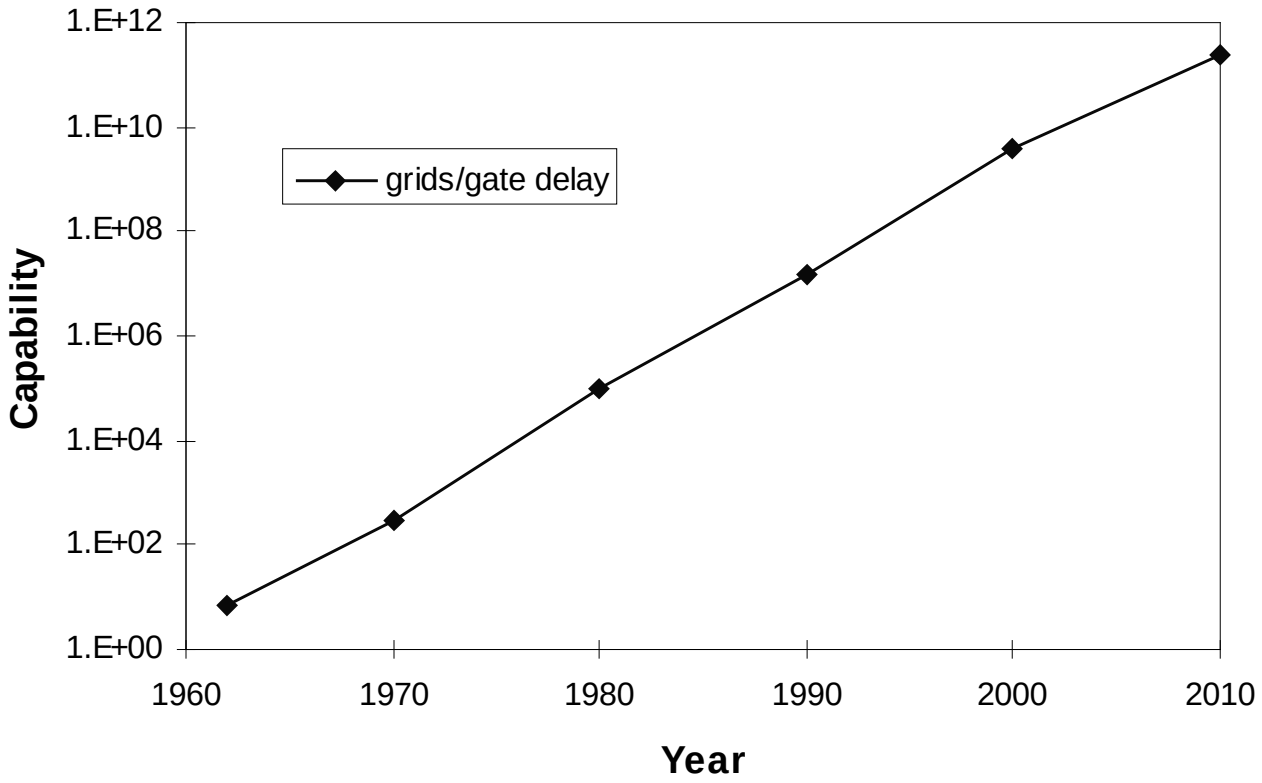
Available Area and Delay





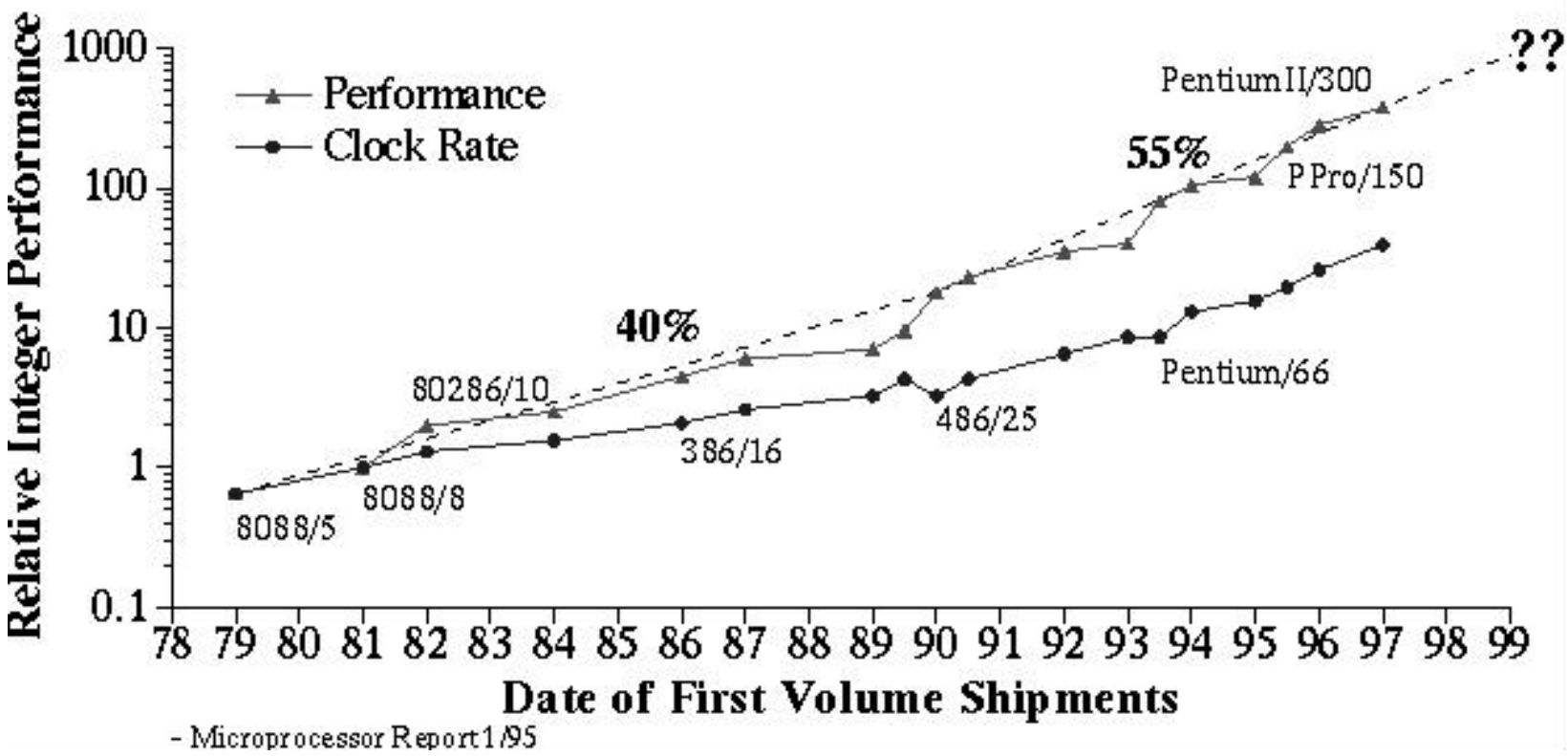
- **Grids up 50%/year, Gate delay down 13%/year**

Chip Capability

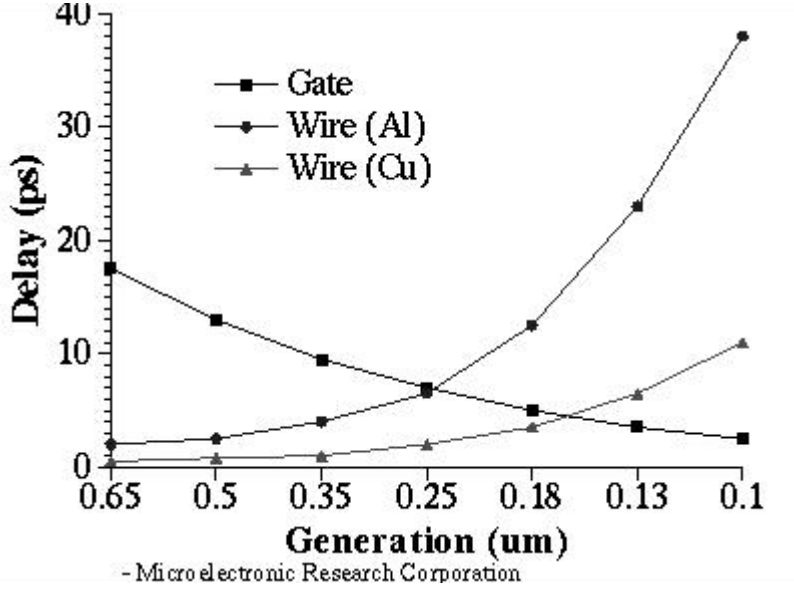


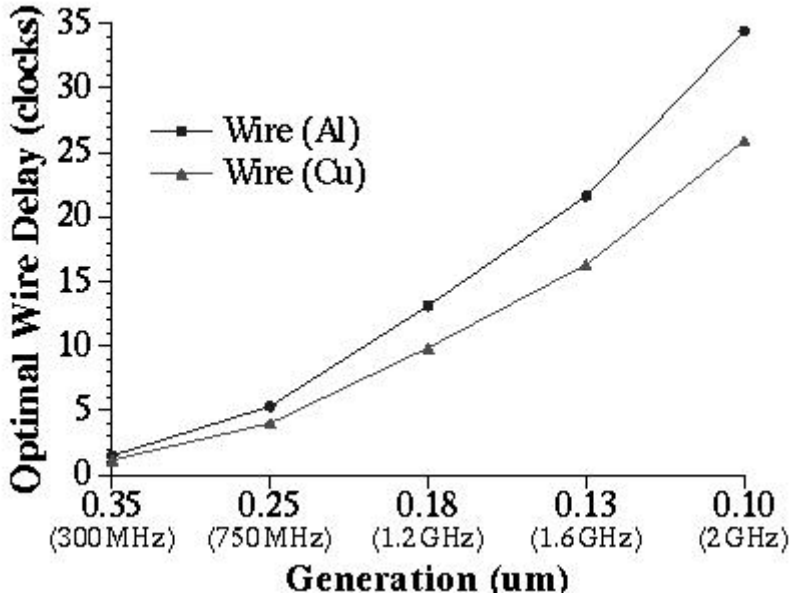
- **Capacity/delay: up 70%/year**

Performance Trends



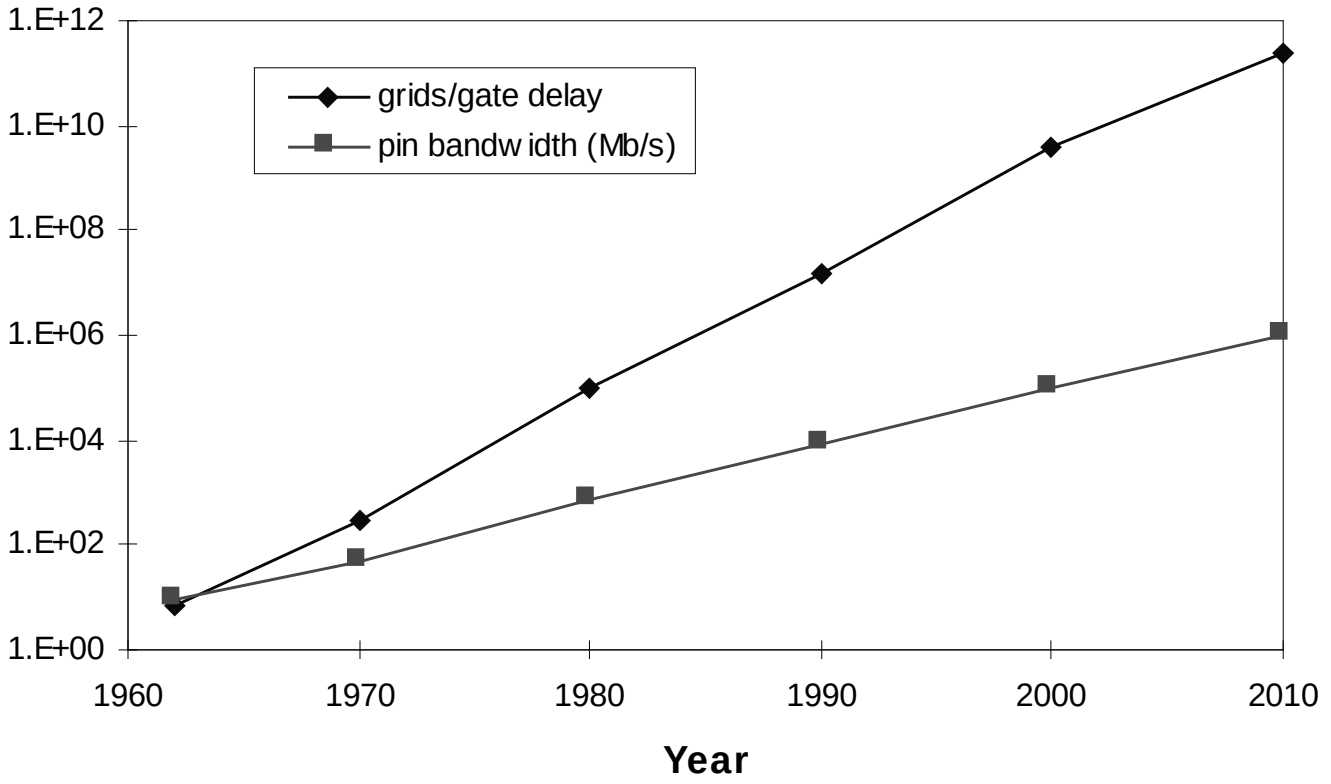
Constraint: Wire Delay





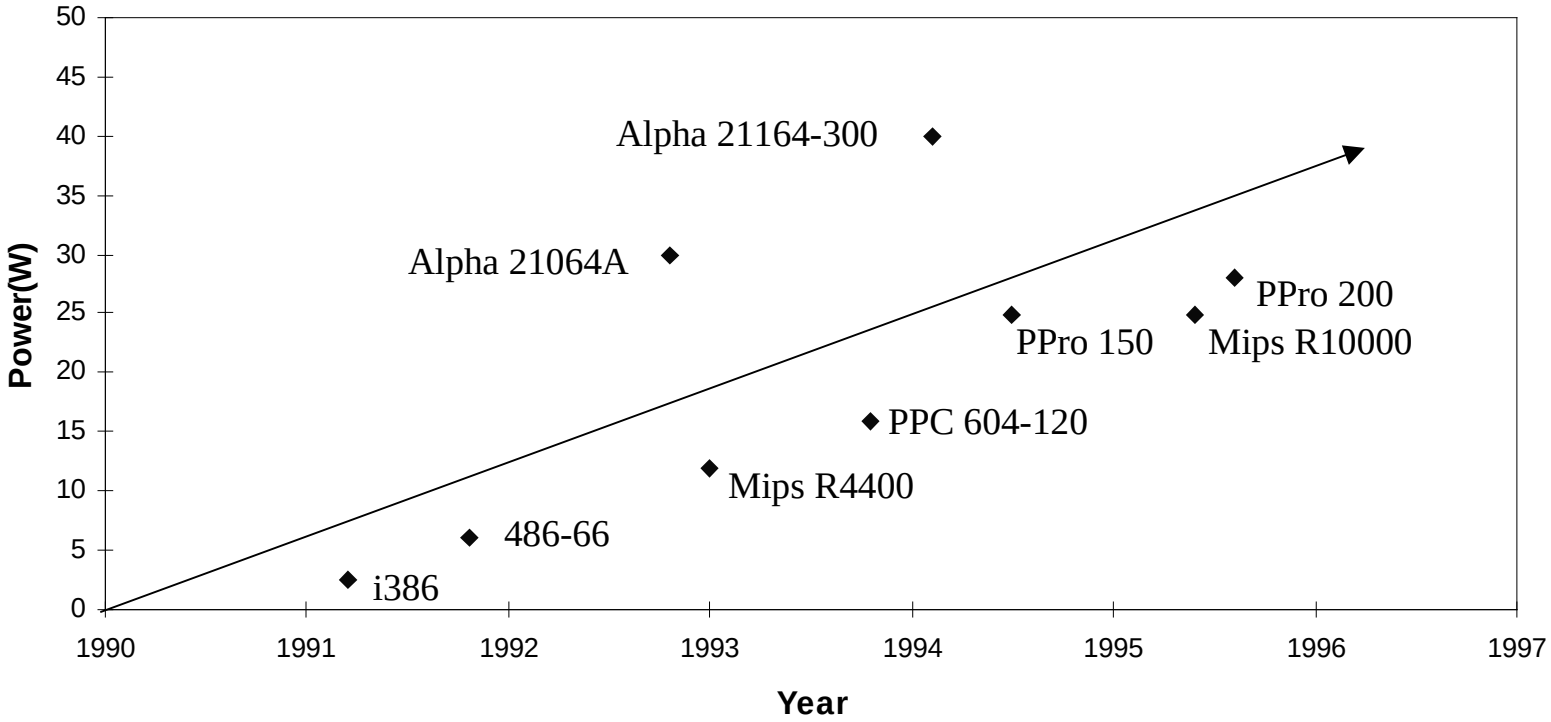
- **Wire delay up 100%/generation**
- **10's of clocks to cross chip in 0.1um process**

Constraint: Pin Bandwidth



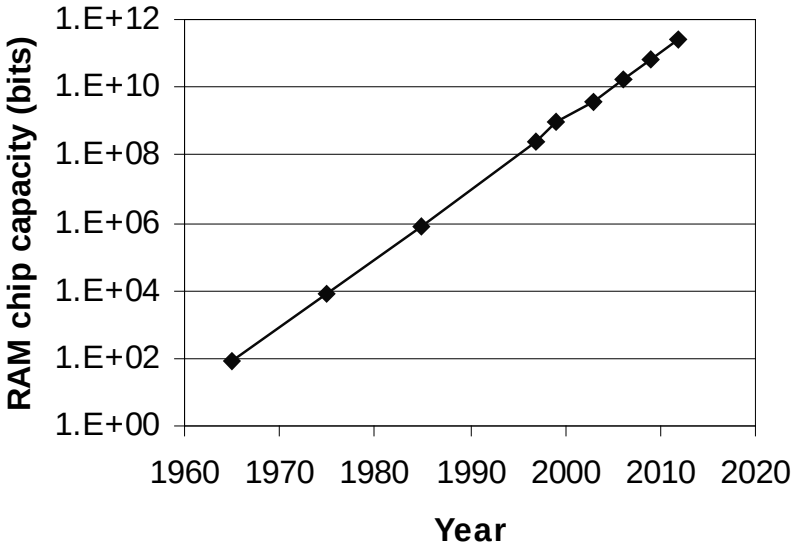
- **Capability up 70%/year, BW up 28%/year**

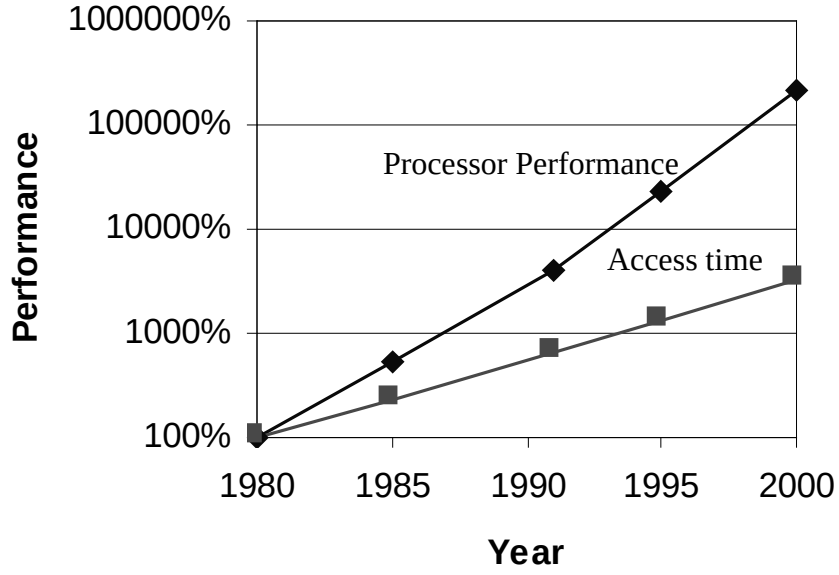
Constraint: Power



- **2X Performance ⟶ 2X Power**

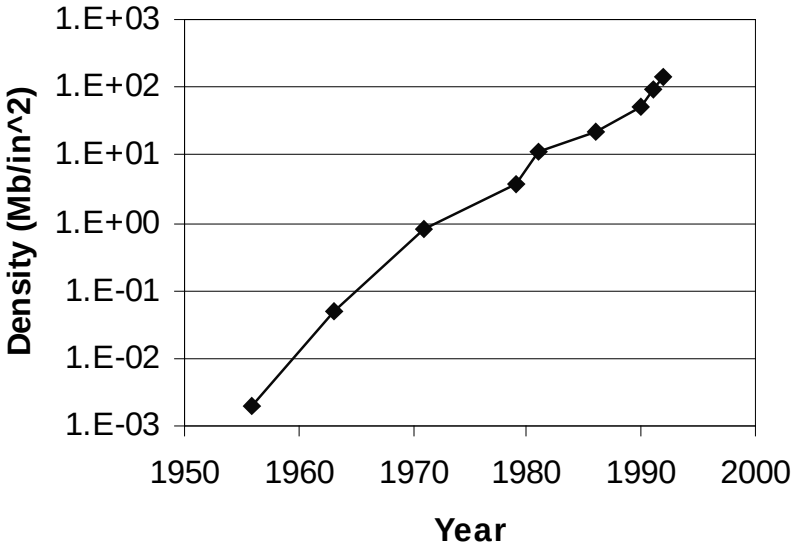
Constraint: DRAMs

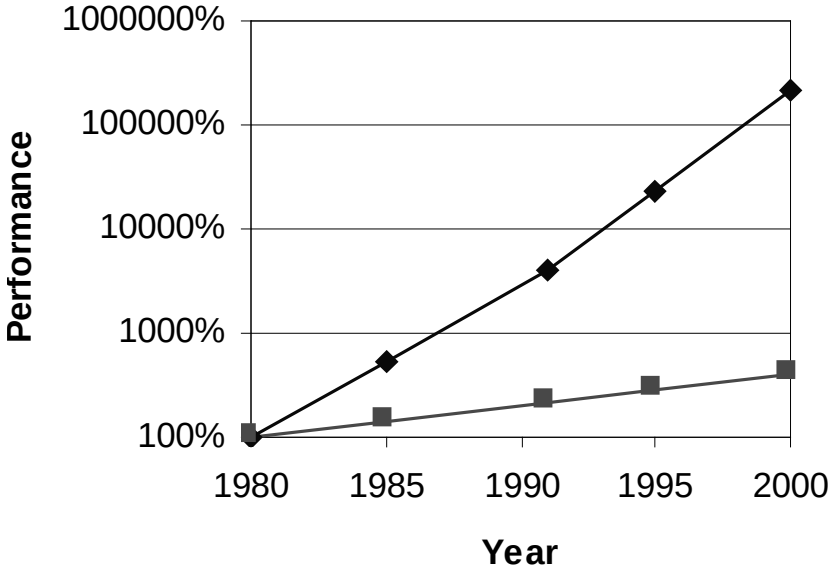




- **Capacity up 60%/year**
- **Access time up 19%/year**

Constraint: Disk Access



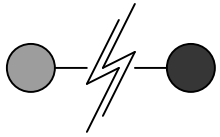


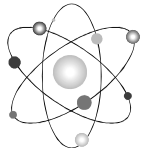
- **Density up 39%/year**
- **Access (seek) time up 7%/year**

Summary

- Exponential improvement from technology
- "Supercomputer" ⟶ Micros
- Future Challenges

Wire delay


Bandwidth


Power

Storage

EXTRA: Read More About It!

- **“Computer Structures: Principles and Examples”, Sieworek, Bell, and Newell, McGraw Hill.**
- **“Computer Technology and Architecture: An Evolving Interaction”, Hennessy and Jouppi, Computer 9/91.**
- **“Digital Systems Engineering”, Dally and Poulton, Cambridge University Press.**
- **“Computer Architecture: A Quantitative Approach”, Hennessy and Patterson, Morgan Kaufman.**