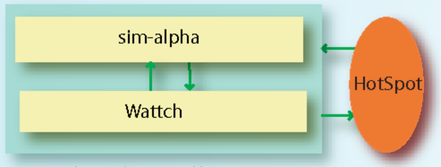
Coordinated Manager for Power, Energy, and Temperature

Motivation

Power constraints can limit microprocessor performance, and power liability is growing due to more transistors and increased leakage currents. Future processor generations will require effective of power management, as well as temperature and energy considerations in order to ensure safe operating condions while mitigating performance limitations. My dissertation research addresses the challenge of next-generation power management with a coordinated power, energy, temperature manager.

Simulation Infrastructure

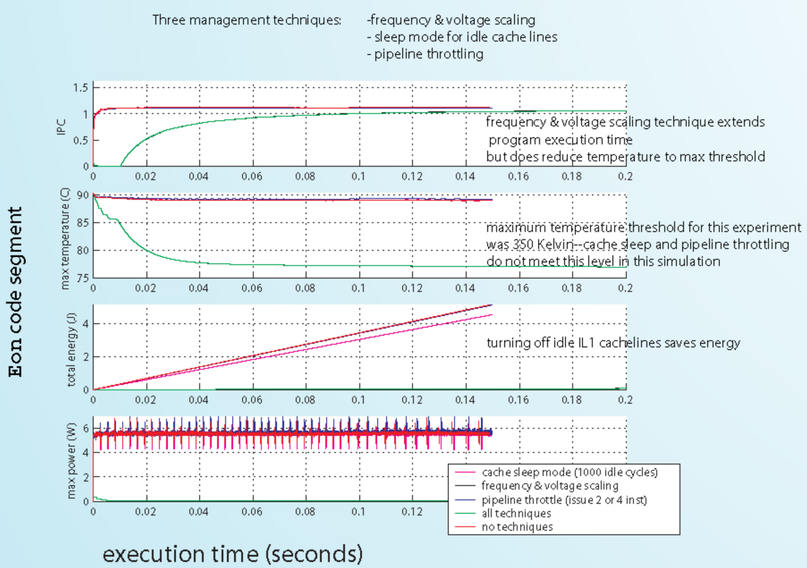


architectural simulation tools

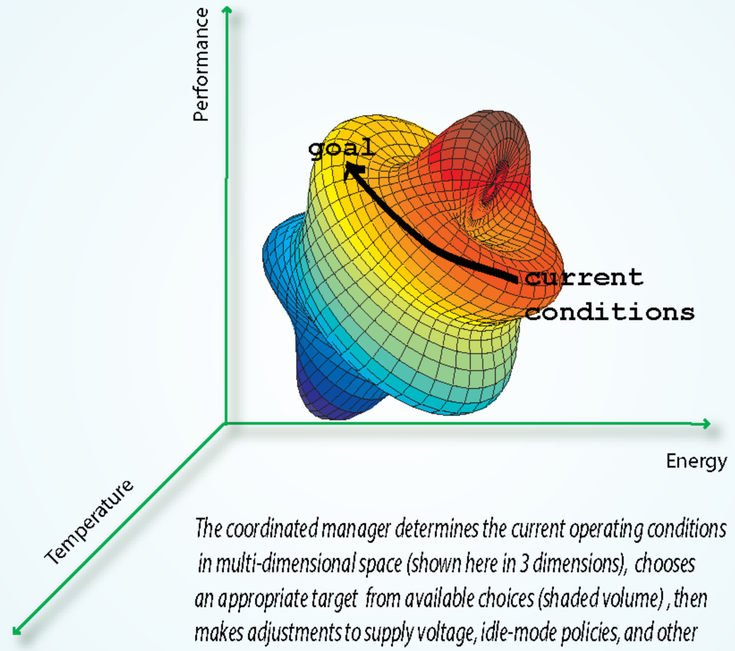
power estimator integrated into performance simulator

temperature estimator

simultaneous measurements for power/energy, temperature, performance



Continuous Optimization



The coordinated manager determines the current operating conditions in multi-dimensional space (shown here in 3 dimensions), chooses an appropriate target from available choices (shaded volume) , then makes adjustments to supply voltage, idle-mode policies, and other management knobs to direct the chip toward its goal operating conditions. The manager continuously monitors the effect of adjustements to tune the result and collects meta-information to re-evaluate the desired goals.

Research Project

Heather Hanson, graduate student
Department of Electrical & Computer Engineering

Stephen W. Keckler, advisor
Department of Computer Sciences

This research is supported by IBM and the Defense Advanced Research Projects Agency under contract F33615-01-C-1892.

Design Overview

The coordinated manager's core algorithm handles multi-criteria decisions to balance requirements for performance, power, energy, temperature.

- goal-driven decisions, rather than fixed policies

- continuous feedback to adjust settings

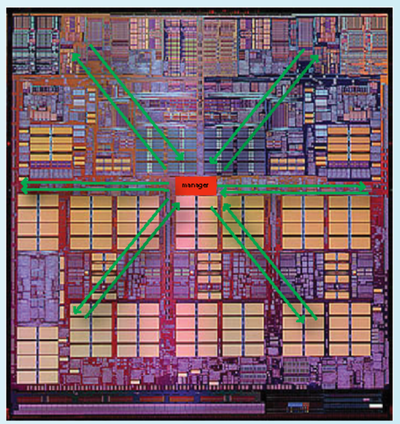
- control distributed between hardware and software to handle monitoring and response time constants

Implementation Ideas

- **embedded processor**, similar to a service processor, to handle decision algorithm calculations and monitoring functions

- **temperature sensors** and **performance counters** send monitoring information

-a **hierarchy** of coordinated control units on processor chips can communicate with higher-level managers on boards and systems



Power4 die photo with superimposed manager

References

- D. Brooks, M. Martonosi, "Wattch: A Framework for Architectural-Level Power Analysis and Optimizations", Proceedings of the 27th Annual Symposium on Computer Architectue, pages 83-94, 2000.

- K. Skadron, M. R. STan, W. Huang, S. Velusamy, K. Sankaranarayanan, D. Tarjan, "Temperature-aware Microarchitecture", Proceedings of the 30th International Symposium on Computer Architecture, pages 2-13, 2003.

- R. Desikan, D. Burger, S.W. Keckler, "Measuring experimental error in microprocessor simulation", Proceedings of the 28th Annual Symposium on Computer Architecture, pages 266-277, 2001.

- H. Hanson, S.W. Keckler, D. Burger, "Coordinated Power, Energy, and Temperature Management for High-Performance Microprocessors", Proceedings of the ACAS conference, 2004.
- example volume from Matlab spharm2